

## EFFICIENCY POTENTIAL ANALYSIS OF P- AND N-TYPE EPITAXIALLY GROWN SI WAFERS

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**ABSTRACT:** In this paper, we investigate the quality of epitaxially grown, 110  $\mu\text{m}$  thick, n- and p-type silicon (Si) layers deposited in a CVD batch reactor of microelectronic standard. Two types of wafers are characterized: ‘EpiRef’ grown on chemically and mechanically polished reference substrates and ‘EpiWafer’ grown on substrates with a porous silicon detachment layer. EpiRef wafers exhibit excellent minority carrier lifetimes of 2.5 ms for n-type and 1.3 ms for p-type. EpiWafers show reduced, but still promising lifetimes of 0.5 ms (in local areas up to 1 ms) for n-type and 40  $\mu\text{s}$  for p-type. For EpiWafers, we found that quality limitations are due to stacking faults as well as interstitial iron contamination for p-type. An efficiency limiting bulk recombination analysis (ELBA), allows for an assessment of the corresponding efficiency potential assuming a TOPcon cell model with a cell limit of 25.9 % for n-type and a TOPCoRE cell model with a cell limit of 26.5 % for p-type. In selected 1  $\text{cm}^2$  areas, potential efficiencies of EpiRef wafers are only -0.4 %<sub>abs</sub> below the theoretical cell limit for n-type and -1.3 %<sub>abs</sub> for p-type whereas EpiWafers feature losses of -1.2 %<sub>abs</sub> for n-type and even -5.4 %<sub>abs</sub> for p-type.

**Keywords:** Epitaxy, Porous Silicon, Photoluminescence Imaging, Efficiency Potential

### 1 INTRODUCTION

In a silicon photovoltaic module, the CZ wafer contributes to  $\approx 30\%$  of the total costs and to  $\approx 40\%$  of the global warming potential (GWP) [1, 2]. The transfer from crystallized CZ wafers to epitaxially grown Si wafers on reusable substrates with a porous silicon detachment layer (EpiWafers) is therefore a sustainable approach to significantly reduce material and energy consumption and thereby costs and GWP. However, in the EpiWafer community, the origin of quality limitation compared to crystallized CZ Si wafers is still under discussion [3–8]. Hence, we analyze quality limitations of n- and p-type epitaxial layers on chemically and mechanically polished (CMP) substrates as reference ‘EpiRef’ in comparison to n- and p-type EpiWafers. We specifically highlight differences between EpiRef wafers and EpiWafers as well as differences between n-type and p-type epitaxially grown silicon.

The main parameter to monitor the material quality is the minority carrier lifetime measured by means of lifetime calibrated photoluminescence imaging (PLI) and quasi steady state photoconductance (QSSPC) [9, 10]. Lifetime losses originate potentially from metal contamination which has its origin in the gas phase or in the sample holder during epitaxial growth as well as from thermally induced stress during the process. Furthermore, the growth template for epitaxy plays a major role as it can be particle contaminated or not perfectly flat. Especially the electrochemically etched and reorganized templates for EpiWafers can still show unclosed areas or even stressed areas within the detachment layer of porous silicon leading to crystal defects during growth [11]. In order to investigate all these lifetime limitations for n- and p-type epitaxially grown Si, we use a two-step approach: First, we characterize EpiRef wafers since their limitations can be directly attributed to contaminations of the gas phase or the sample holder, or to thermally induced stress during the process. Second, these EpiRef wafers are compared to EpiWafers since the additionally arising quality limitations can be attributed to properties of the reorganized template.

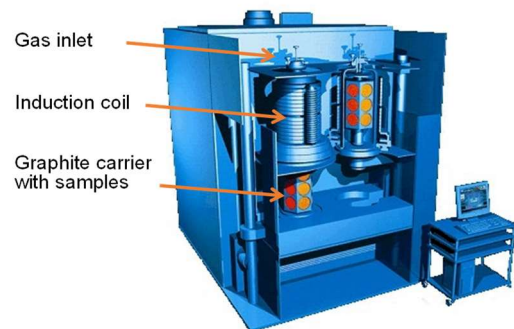
In addition to the lifetime measurements, efficiency limiting bulk recombination analysis (ELBA) allows to discuss the impact of quality limiting effects on solar cell

efficiency. For the spatially resolved efficiency potential analysis based on infection dependent PLI measurements, we assume a TOPcon model for n-type epitaxial layers and a TOPCoRE model for p-type epitaxial layers [12].

### 2 EXPERIMENTAL PROCEDURE

#### 2.1 Epitaxial growth of silicon

The epitaxial growth of Si is conducted in a chemical vapor deposition (CVD) batch reactor from LPE (PE 2061S), called ‘PEpi’, by using  $\text{SiHCl}_3$  and  $\text{H}_2$  as precursor gases. For adjustable p- and n-type doping,  $\text{B}_2\text{H}_6$  and  $\text{PH}_3$  gases can be added to the precursors. The gas flows are adjusted to grow Si layers with thicknesses of 130  $\mu\text{m}$  after 140 min of deposition (growth rate  $\approx 1 \mu\text{m}/\text{min}$ ) at process temperatures between 1090  $^\circ\text{C}$  and 1120  $^\circ\text{C}$ . The chosen doping concentration of the n-type layers is approximately  $3.5 \times 10^{15} \text{ cm}^{-3}$  ( $\approx 1.4 \Omega\text{cm}$ ) and for p-type layers it is  $4.7 \times 10^{15} \text{ cm}^{-3}$  ( $\approx 3.0 \Omega\text{cm}$ ). Figure 1 shows a schematic of the PEpi pointing out the gas inlets, the induction coil and the silicon carbide coated graphite carrier holding the wafers in a vertical position. The excellent thermal and gas flow stabilities lead to a spatially homogeneous thickness and a low stress level of the epitaxial layer as well as to adjustable and homogeneous doping concentrations over the whole layer depths [13].

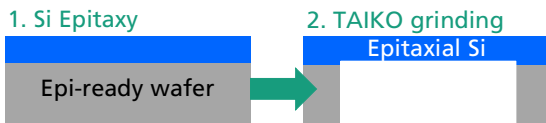


**Figure 1:** Schematic of the CVD-reactor PE2061 (“PEpi”) used for high quality epitaxy.

## 2.2 Preparation of EpiRef wafers

For obtaining EpiRef wafers, n-type, respectively p-type Si is deposited on 6" CZ Si p-type substrates with chemically mechanically polished (CMP), 'epi-ready' surfaces on microelectronic quality level supplied by Siegert. The substrate's thickness is 675  $\mu\text{m}$  and its resistivity is (1-10)  $\Omega\text{cm}$ . After epitaxial growth, the CZ substrate is locally removed through Taiko-grinding (by the external service provider DISCO). Grinding residues are taken off by KOH etching resulting in an exclusively epitaxial layer with a wafer thickness of 110  $\mu\text{m}$  and a CZ-rim for stability as demonstrated in

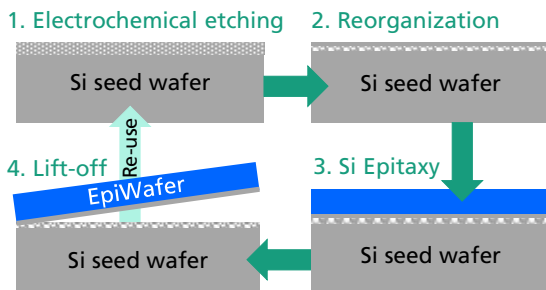
Figure 2 For further lifetime measurements, the EpiRef wafers are cleaned by RCA procedure, passivated with  $\text{Al}_2\text{O}_3$  and forming gas annealed at 425  $^\circ\text{C}$ .



**Figure 2:** EpiRef wafer scheme: 1. Silicon deposition on an epi-ready wafer in PEpi reactor. 2. Taiko-grinding of the substrate so that only the epitaxial silicon remains in the inner, circular area.

## 2.3 Preparation of EpiWafers

The EpiWafers are epitaxially grown on Si seed wafers with porous silicon layer stacks supplied by IMS. These seed wafers are 6" CZ Si p<sup>+</sup>-type substrates with a resistivity of (10-20) m $\Omega\text{cm}$  and a thickness of 650  $\mu\text{m}$ . Figure 3 shows the whole process starting from the seed wafer with an electrochemically etched sponge-like silicon layer underneath the surface. This layer is reorganized during a 5 min high-temperature step at 1120 $^\circ\text{C}$  under  $\text{H}_2$  atmosphere in the PEpi reactor forming a high porous detachment layer and a closed surface acting as template for epitaxial growth. Then, Si is deposited with the same setting as for the EpiRef samples. Finally, after edge definition with a chip saw, 5x5  $\text{cm}^2$  pseudo-square EpiWafers can be lifted off the seed wafer by using a vacuum lift-off tool. For the characterization, the EpiWafers are prepared by KOH etching to remove residuals of the porous silicon seed wafer, again leading to 110  $\mu\text{m}$  wafer thickness. Finally, RCA cleaning, passivation with  $\text{Al}_2\text{O}_3$  and forming gas anneal at 425  $^\circ\text{C}$  follows.



**Figure 3:** EpiWafer scheme: 1. Electrochemical etching of Si seed wafer. 2. Reorganization process to create porous detachment layer. 3. Silicon epitaxy. 4. Lift-off of EpiWafer from seed wafer.

## 2.4 Lifetime and efficiency potential characterization

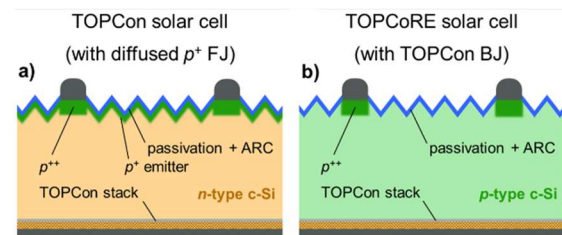
Spatially resolved lifetime images were determined by photoluminescence imaging (PLI) calibrated with modulated photoluminescence at a range of illumination intensities from 0.001 to 2.5 suns [9, 10]. Thus, injection levels of all relevant solar cell operation conditions are covered. At an injection level of 0.05 suns (approximately injection level at maximum power point) the lifetime value  $\tau_{\text{eff}}$  of the whole wafer was obtained by arithmetic averaging. Additionally, injection-dependent, but not spatially resolved, lifetimes were detected by quasi steady state photoconductance (QSSPC).

In a semi-simulative approach the cell efficiency potential was quantified by efficiency limiting bulk recombination analysis (ELBA) based on injection dependent and spatially resolved lifetime data combined with pixelwise numerical cell simulations with Quokka 3 applying a 2D unitcell model [14, 15]. The selected solar cell models are further described in chapter 2.5. Finally, the global solar cell parameters can be calculated by applying the concept of Isenberg *et al.* on the local electrical quantities [16]. The efficiency evaluation was applied to specific regions of interest: an area covering almost the whole wafer and a smaller best performance area with the size of 1  $\text{cm}^2$ .

For further insights into the origin of differences in lifetimes between the wafer types, we performed iron imaging and defect counting considering stacking faults as well as decorated stacking faults with poly-crystalline inclusions leading to a further reduction in lifetime than ordinary stacking faults [17].

## 2.5 Cell Models for ELBA

For ELBA analysis, we chose two state-of-the-art high efficiency cell models which are depicted in Figure 4 and fully described in detail by Richter *et al.* [12]. In our case, the n-type TOPCon cell can reach an efficiency cell limit of  $\eta_{\text{Limit}} = 25.9\%$  and the p-type TOPCoRE with an efficiency cell limit of  $\eta_{\text{Limit}} = 26.5\%$ . These limits assume only intrinsic recombination without any defect related recombination in the base material. Both cell models use similar fabrication technologies with a TOPCon stack at the rear surface and highly doped p<sup>++</sup>-regions underneath the front metal contact. The main difference is the location of the junction: p<sup>+</sup>-doped front junction (FJ) at the n-type Si cell and TOPCon back junction (BJ) without a front surface field (FSF) at the p-type Si cell. Thus, the back junction requires higher material quality (diffusion length) to avoid significant efficiency losses within a p-type TOPCoRE cell.



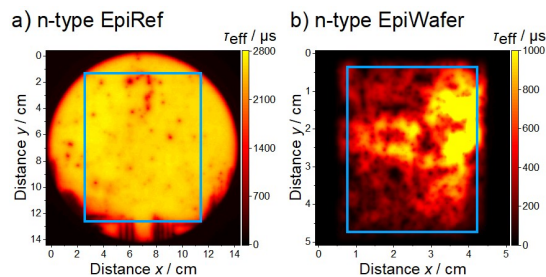
**Figure 4:** Schematic of cell models used in ELBA: a) TOPCon at the rear surface and n-type Si cell with an  $\text{Al}_2\text{O}_3$ -passivated, boron-doped p<sup>+</sup> FJ, b) TOPCoRE p-type Si cell with an  $\text{Al}_2\text{O}_3$  passivation of the bare c-Si front surface without a full-area FSF, with highly doped p<sup>++</sup> regions underneath the front metal contact and a TOPCon BJ [12].

### 3 LIFETIME RESULTS

#### 3.1 n-type epitaxial layer

In this section, the focus lies on the electrical characterization by means of PLI and QSSPC of n-type EpiRef grown on a substrate with CMP surface and n-type EpiWafer grown on substrate with porous silicon detachment layer.

In Figure 5, lifetime mappings detected by PLI at an illumination of 0.05 suns are shown. The blue frames in both images mark the areas in which we calculated a lifetime mean value  $\tau_{\text{eff}}$  of  $(2.5 \pm 0.2)$  ms for the EpiRef wafer and  $(0.5 \pm 0.3)$  ms for the EpiWafer. The lifetime distribution of the EpiRef wafer is very homogeneous. Only some stacking faults (dark spots) and some slip lines (horizontal and vertical lines) are visible. These minor areas of lower lifetimes originate mainly from gas phase contamination, such as oxygen residuals, and from local thermal inhomogeneities. In contrary, the EpiWafer shows an inhomogeneous spatial lifetime distribution with many spots of locally deviating lifetime manifesting itself also in the large standard deviation of the mean lifetime. The lifetime reduction in comparison to EpiRef is mainly attributed to the increased amount of stacking faults ( $> 100 \text{ cm}^{-2}$  for the EpiWafer vs.  $< 1 \text{ cm}^{-2}$  for the EpiRef). The lower crystal quality can be explained by the epitaxial growth of the EpiWafer on the non-ideally reorganized porous silicon template with surface steps or even holes in the template. However, it is remarkable that the EpiWafer has local areas with very promising lifetime up to 1 ms without any additional gettering process step which shows the potential of EpiWafers.

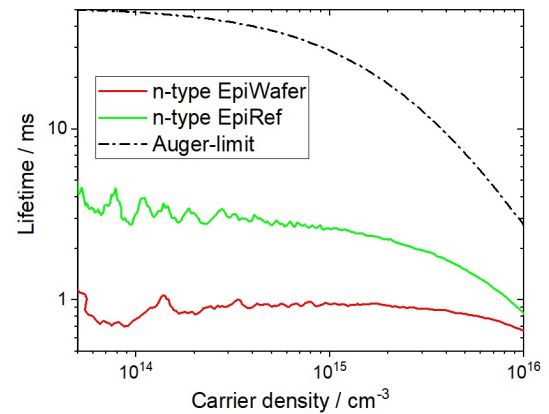


**Figure 5:** Lifetime detected by PLI at 0.05 suns with blue frames marking the area for the average lifetime  $\tau_{\text{eff}}$  and for efficiency potential analysis. a) n-type reference wafer with 2.5 ms average lifetime. b) n-type EpiWafer with 0.5 ms average lifetime.

QSSPC measurements in Figure 6 confirm that the EpiRef shows higher lifetimes than the EpiWafer although the lifetime for the EpiWafer is overestimated caused by an overweighting of regions with excellent lifetimes on wafers with inhomogeneous lifetimes. Both wafers exhibit relatively stable lifetimes over the hole carrier density range despite of large carrier densities where the lifetime is additionally reduced due to Auger recombination. Further, detected lifetimes are more than ten times below the Auger-limit implying recombination due to contamination in both, EpiRef and EpiWafer as discussed in detail for the p-type wafers in Chapter 3.2.

Reasons for the lifetime reduction of the EpiWafer in comparison to the EpiRef are still discussed and investigated. Besides the non-ideally reorganized surface of the seed wafer, the p<sup>+</sup>-doping of the seed wafers potentially further reduces the quality of the EpiWafer. We

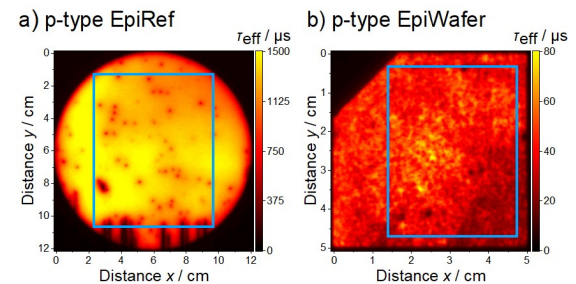
measured a severe reduction of lifetime by about 50% of EpiRef wafers grown on highly doped p<sup>+</sup>-type epi-ready substrates compared to p-type epi-ready substrates. This reduction is either attributed to an increased metal contamination due to the higher boron content of the substrate, as the boron source is less pure than the silicon source, or attributed to a lattice mismatch between the p<sup>+</sup>-substrate and the p-type EpiWafer due to different atomic radii of dopants and silicon [18]. Furthermore, we cannot exclude that the EpiWafer is exposed to additional contamination from more handling steps of the seed wafer before epitaxy compared to the template of the EpiRef as every additional handling step poses a source of potential contamination and surface damage.



**Figure 6:** Lifetime curves measured by QSSPC of n-type EpiRef wafer and EpiWafer as well as the Auger-limit for 1.4 Ωcm n-type silicon [19].

#### 3.2 p-type epitaxial layer

In this section, we analyze p-type EpiRef wafer and EpiWafer and point out differences between n- and p-type epitaxial silicon. Similar to the n-type epitaxial layer, there is a significant reduction of lifetimes from p-type EpiRef to EpiWafer. The PLI measurements in Figure 7 exhibit mean lifetime  $\tau_{\text{eff}}$  within the area marked by the blue frame of  $(1.3 \pm 0.2)$  ms for EpiRef and  $(0.04 \pm 0.01)$  ms for EpiWafer.



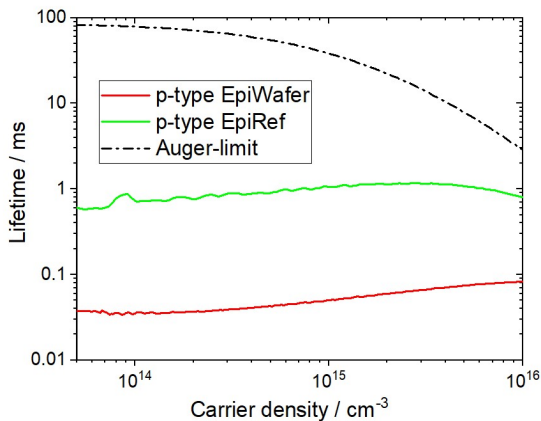
**Figure 7:** Lifetime detected by PLI at 0.05 suns with blue frames marking the area for the average lifetime  $\tau_{\text{eff}}$  and for efficiency potential analysis. a) p-type EpiRef with 1.3 ms average lifetime. b) p-type EpiWafer with 0.04 ms average lifetime.

Again, the EpiRef has a reasonably smooth lifetime distribution over the whole wafer area with little amount of slip lines and stacking faults whereas the EpiWafer appears more spatially inhomogeneous. Same as for n-type wafers, defect counting unveils a large difference in

stacking fault density of  $> 100 \text{ cm}^{-2}$  for the EpiWafer and  $< 1 \text{ cm}^{-2}$  for the EpiRef. Hints for decorated stacking faults, which show even higher recombination activity, on EpiWafers were found on microscope images of the layer surface.

Same as for the n-type layers, results of QSSPC measurements on p-type layers in Figure 8 are consistent with PLI. Again, the detected lifetimes depend only little on the carrier density, which means that the PLI results are valid for a wide range of injection levels. For p-type, the lifetimes are even more than 100 times below the Auger-limit, indicating again recombination through contamination. For the p-type EpiWafer, iron imaging confirms an enhanced metal contamination showing an interstitial iron concentration  $Fe_i$  in the range of  $10^{10} \text{ cm}^{-3}$ . In contrast, the interstitial iron concentration of the EpiRef appears to be below the detection limit of  $5 \times 10^9 \text{ cm}^{-3}$ . However, the interstitial iron contamination only makes up for less than 10 % of the total recombination within the p-type EpiWafer. Therefore, other metallic contaminations are assumed to contribute to the recombination, especially for the EpiWafers.

Generally, lifetimes are reduced for p-type wafers compared to n-type wafers. For the EpiRef wafer the lifetime decreases by a factor of two and for the EpiWafer even by a factor of ten as summarized in Table I in chapter 4.1. Several reasons for lower lifetimes in p-type Si epitaxial layers than n-type Si epitaxial layers exist. For example, iron contamination has a larger impact on minority carrier lifetimes in p-type silicon because the capture cross section of interstitial iron is much larger for electrons than for holes [20]. Since the detected interstitial iron content does not fully explain the lifetime reduction, further research on other metallic contamination is ongoing. However, the lower minority carrier lifetimes in p-type silicon does not necessarily have to lead to lower cell efficiencies since the lifetime dependent diffusion length of p-type EpiRef with  $D = 2.0 \text{ mm}$  is in the same order as the even slightly smaller diffusion length of n-type EpiRef with  $D = 1.7 \text{ mm}$  due to the larger mobility of electrons in p-type silicon [21].

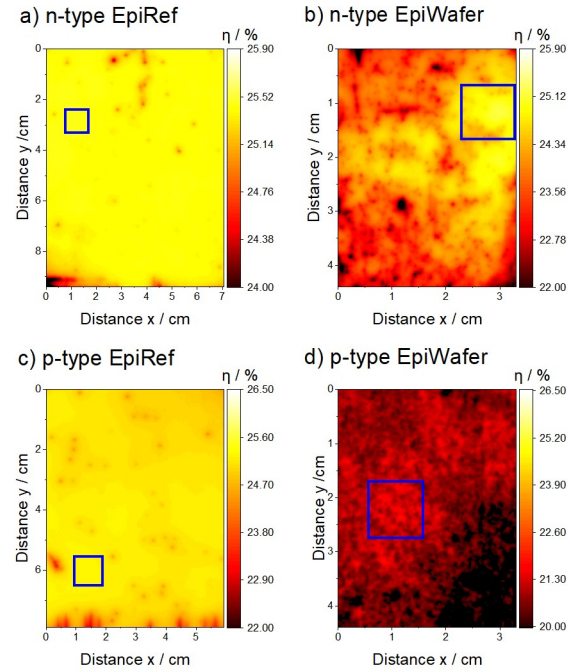


**Figure 8:** Lifetime curves measured by QSSPC of p-type EpiRef wafer and EpiWafer as well as the Auger-limit for 3 Ωcm p-type silicon [19].

## 4 EFFICIENCY POTENTIAL ANALYSIS

### 4.1 ELBA simulation results

In Figure 9, we show the cell efficiency potential of the epitaxially grown layers according to method ELBA described in section 2.4. To compare all wafer types with each other, we define two areas of interest: a large rectangular area (full depicted area) and a second smaller 1 cm<sup>2</sup> area covering the best minority lifetimes. The n-type EpiRef wafer reaches 25.4 % efficiency on a large scale and 25.5 % in the best spot whereas the n-type EpiWafer reaches 23.8 % efficiency on a large scale and 24.7 % in the best spot. Slightly lower results are obtained for the p-type EpiRef wafer with 25.0 % efficiency at large size and 25.2 % for the small 1 cm<sup>2</sup> spot. A tremendous reduction in efficiency potential is observed for the p-type EpiWafer with 20.6 % on large area and 21.1 % efficiency at the best location. These results are listed in direct comparison to the lifetime results in Table I.

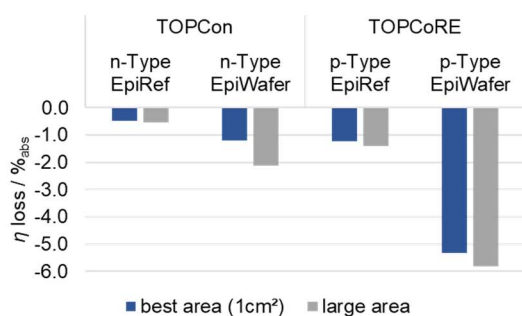


**Figure 9:** ELBA simulation results predicting the lateral distributed cell efficiency  $\eta$  for different wafers. Further evaluated areas are depicted:  $\eta_{\text{Best}}$  best performance area (1 cm<sup>2</sup>) indicated by the blue box,  $\eta_{\text{Wafer}}$  at the full depicted wafer area (indicated by the blue box in Figure 5 and Figure 7).

**Table I:** Evaluation results of material and cell performance parameters. PLI at 0.05 suns intensity for mean lifetimes  $\tau_{\text{eff}}$  (arithmetic mean) and diffusion lengths  $D$ . ELBA simulation results for cell efficiencies  $\eta$  evaluated at a large area and a best 1 cm<sup>2</sup> area.

	$\tau_{\text{eff}}$ ms	$D$ mm	$\eta_{\text{Limit}}$ %	$\eta_{\text{Best}}$ %	$\eta_{\text{Wafer}}$ %
n-type EpiRef	2.5	1.7	25.9	25.5	25.4
n-type EpiWafer	0.5	0.8	25.9	24.7	23.8
p-type EpiRef	1.3	2.0	26.5	25.2	25.0
p-type EpiWafer	0.04	0.4	26.5	21.1	20.6

The efficiency loss  $\eta_{\text{loss}}$  is given in Figure 10 by comparing the simulated solar cell efficiency  $\eta$  with the specific solar cell limit  $\eta_{\text{Limit}} = 25.9\%$  for n-type and  $\eta_{\text{Limit}} = 26.5\%$  for p-type material. The inhomogeneity within a wafer is represented in the difference between the bars (blue for the best area vs. gray for the large area). This difference is very prominent for the n-type EpiWafer compared to the n-type EpiRef. Again, a tremendous efficiency loss is visible for the p-type EpiWafer with over  $-5\%$ abs. In general, there are small efficiency losses between the large area and the best area in the group of EpiRef wafers corresponding to the reasonably good lifetime homogeneity over the whole EpiRef wafers. Further, the p-type material is on a reduced quality level compared to n-type material for these cell models despite of the longer diffusion length for p-type EpiRef than for n-type EpiRef. However, especially the potential efficiencies for EpiRef wafers indicate, that epitaxially grown n- and p-type silicon layers in the ‘PEpi’-reactor are promising candidates for base material for high efficiency cell models. Their calculated efficiencies suggest that high efficiency cells out of our epitaxial layers could exceed efficiencies of industrially produced cells out of crystallized CZ-material [2]. Efficiencies of high-end high efficiency cells out of crystallized FZ-material cannot fully be reached with our epitaxial layers yet [12].



**Figure 10:** Evaluation summary of efficiency losses based on ELBA simulations (shown in Figure 9). The losses are given in absolute values, referenced to the corresponding cell limits with  $\eta_{\text{Limit}} = 25.9\%$  for n-type and  $\eta_{\text{Limit}} = 26.5\%$  for p-type material.

#### 4.2 Limitations of the conducted efficiency analysis

As the observed material is in an intermediate processing state, there is an uncertainty relative to the final material quality which could be influenced by further treatment steps such as high temperature processes, chemical etching, emitter diffusion, and metallization. These treatment steps could influence the material quality in a positive but also negative way. The selection of an appropriate cell model is another challenge: to fully lift the potential of highly efficient cell models, in specific TOPCoRE, high-quality bulk material is required. Further the material’s doping concentration and layer thickness influences the cell limit as well as the potential cell efficiency. In this contribution, both parameters were not optimized for the applied cell model which might offer room for further improvements.

## 5 CONCLUSION

In this contribution, qualities of n- and p-type EpiRef wafers and EpiWafers were compared. For EpiRef wafers,

we achieved remarkable minority carrier lifetimes of 2.5 ms and a predicted cell efficiency potential of 25.4 % for n-type Si (TOPCon model with cell limit of 25.9 %) and 1.3 ms mean lifetime, with 25.0 % efficiency for p-type Si (TOPCoRE model with cell limit of 26.5 %). This confirms the high quality of the epitaxially grown layers for both, n- and p-type Si, and the excellent level of purity in the CVD-reactor ‘PEpi’. EpiWafers feature lower minority carrier lifetimes than EpiRef wafers which is attributed to the influence of the highly doped seed wafer with a porous silicon detachment layer used for growing EpiWafers. The lifetime reduction for EpiWafers corresponds to a higher amount of stacking faults and a detectable iron contamination compared to EpiRef wafers grown on epi-ready surfaces. Furthermore, other metallic contaminations are assumed and will be investigated in the future. These results underline the urgent need of seed wafers with low contamination level and a smooth and homogeneous porous silicon detachment layer as well as the importance of further research on the influence of lattice- and doping concentration mismatch between epitaxial layer and seed wafer. In direct comparison between n-type and p-type silicon, n-type EpiWafers and EpiRef wafers exhibit longer lifetimes and higher efficiency potentials than p-type wafers. The explanation for the noteworthy difference is not yet found in detail. Generally, p-type silicon is more prone to certain metallic contaminations than n-type silicon such as interstitial iron. However, lower lifetimes for p-type material can be compensated by longer diffusion lengths due to higher minority carrier mobility and by adjusted cell models. Hence, we achieved encouraging potential cell efficiencies for both, n- and p-type material, for the high efficiency solar cell models TOPCon and TOPCoRE.

## 6 ACKNOWLEDGMENTS

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