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HIGH THROUGHPUT SOLAR CELL PROCESSING BY OXIDATION OF WAFER STACKS

M. Meßmer, S. Lohmüller, F. Braun, J. Weber, A. Wolf
Fraunhofer Institute for Solar Energy System (ISE), Heidenhofstr. 2, 79110 Freiburg, Germany
Phone: +49 761 4588-2287; e-mail: marius.messmer@ise.fraunhofer.de

ABSTRACT: In this work, we investigate two approaches for high throughput emitter formation and thermal oxidation for passivated emitter and rear cells (PERC). The low temperature stack oxidation (LoTSOx) approach uses wafer stacks in the typical low temperature thermal oxidation process in the PERC manufacturing sequence. With the LoTSOx approach, we reach similar energy conversion efficiencies of $\eta = 22.2\%$ in comparison to state-of-the-art PERC processing but with 3.1 times higher throughput. The second approach, using a shortened low pressure $POCl_3$ diffusion and a high temperature stack oxidation (HiTSOx approach) with laser-doped selective emitter, yields a peak conversion efficiency of $\eta = 22.0\%$ and low specific contact resistances $\rho_c \approx 0.6$ mΩcm^2. We further investigate different diffusion and oxidation processes for the HiTSOx approach resulting in a wide range of emitter sheet resistances R_{sh}. We reach low emitter dark saturation current densities of $j_{0e} = 12$ fA/cm^2 at $R_{sh} = 389$ Ω/sq while stacking the wafers during the oxidation process.
Keywords: High throughput, wafer stacks, LP-$POCl_3$ diffusion, thermal oxidation, HiTSOx

1 INTRODUCTION

The passivated emitter and rear cell (PERC) [1, 2] is the mainstream solar cell device structure. According to ITRPV (international technology roadmap) expert survey it is expected to remain in this leading market share position for the coming years [3]. In addition, a significant increase in the production tool throughput is predicted [3]. Several process steps in the fabrication of PERC solar cells must be adapted to reach high throughputs. For this, several approaches are under investigation [4]. The PERC sequence usually incorporates a phosphorus oxychloride ($POCl_3$) diffusion after texturing to form the emitter as well as a low temperature oxidation / annealing process between chemical edge isolation and plasma enhanced chemical vapor deposition (PECVD) for passivation [2]. Newest generations of tube furnaces can process up to 1,600 wafers per process tube.

The aim of this work is to strongly increase the production tool throughput of the thermal processes while maintaining a high solar cell performance. We increase the potential throughput by a factor up to 3.1 by implementation of horizontally stacked wafers during the oxidation process. Two approaches are investigated: (i) the low temperature stack oxidation (LoTSOx) which is based on stacking wafers in the low temperature thermal oxidation process typically used in the PERC sequence as surface passivation, and (ii) the high temperature stack oxidation (HiTSOx) [5, 6] for simultaneous emitter drive-in and surface passivation. For the latter, the diffusion process is adapted. Both approaches are implemented in the PERC fabrication sequence.

2 HIGH THROUGHPUT APPROACHES

2.1 Low temperature stack oxidation LoTSOx

The first approach investigated in this paper is the <u>lo</u>w <u>t</u>emperature <u>s</u>tack <u>ox</u>idation LoTSOx. This approach follows the typical fabrication sequence for PERC solar cells including thermal oxidation like the baseline process at Fraunhofer ISE [2]. Figure 1 depicts the state-of-the-art diffusion process using phosphorus oxychloride ($POCl_3$) as liquid dopant precursor. The subsequent thermal oxidation process features low temperature as mentioned in Ref. [2, 7] and thus hardly affects the doping profile and grows a thin silicon dioxide SiO_2 as a passivation layer. Both processes usually capture 1,600 wafers (M6 configuration). In the LoTSOx approach, a highly increased throughput of more than 5,000 wafers per batch can be achieved by horizontally stacking of the wafers on top of each other, resulting in a 3.1 times higher throughput. It can be used for solar cells with homogeneous or selective emitter.

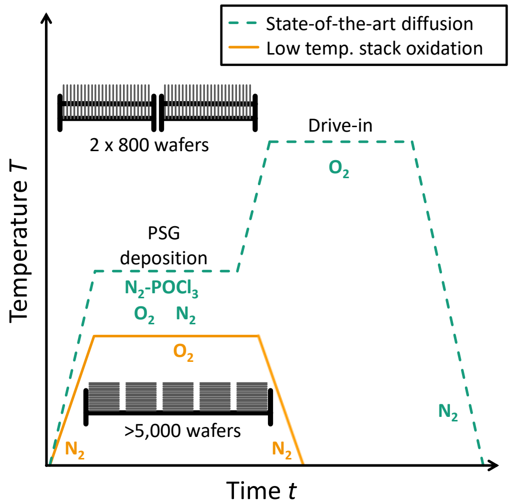

Figure 1: Schematic illustration of the state-of-the-art tube furnace $POCl_3$ diffusion process as a function of the temperature T over time t with a typical process throughput of 1,600 wafers (M6 configuration). Further, the low temperature stack oxidation (LoTSOx) with a throughput of more than 5,000 wafers is illustrated.

2.2 High temperature stack oxidation HiTSOx

The <u>hi</u>gh <u>t</u>emperature <u>s</u>tack <u>ox</u>idation HiTSOx has already been introduced in Ref. [5, 6]. It uses adapted $POCl_3$ diffusion shortened to only the deposition phase. Thereby, the throughput of the diffusion process is increased by a factor of 1.8. Laser doping from this phosphosilicate glass (PSG) layer [8, 9] shows high suitability [5] for the formation of a laser-doped selective emitter (LDSE) and is used for solar cell processing in this work. Homogeneous emitter formation with the HiTSOx approach is also possible but not investigated here. The drive-in of the phosphorus atoms is shifted to the thermal oxidation process where again horizontally stacking of the wafers increases the throughput to more than 5,000 wafers per batch, increasing the throughput by a factor of 2.4. This stack oxidation process features plateau temperatures in the range of typical drive-in temperatures between 850°C < T_{plateau} < 900°C [6]. During this process, the phosphorus incorporated in the silicon is redistributed and diffuses in further. At the same time, a silicon dioxide SiO_2 grows on the wafer surface, which serves as a passivation layer in combination with a hydrogen rich capping layer.

A cost of ownership (COO) calculation for the HiTSOx approach shows a COO reduction of 41% compared to the state-of the art approach [4]. In this calculation, M6 sized wafers and a possible throughput of 1,600 wafers per process tube for state-of-the-art diffusion and thermal oxidation are taken into account.

3 EXPERIMENT

In this investigation, two solar cell batches are manufactured, as depicted in Figure 2. Group A1 and B1 represent the respective reference groups with common PERC fabrication sequence featuring a homogeneous emitter. Group A2 is meant for investigating the low temperature stack oxidation LoTSOx approach as described in section 2.1 and Group B2 the high temperature stack oxidation (HiTSOx) approach as described in section 2.2. For the manufacturing, we use M2 *p*-type boron-doped Cz-Si wafers with a base resistivity of $\rho_b \approx 0.8\ \Omega$cm. An alkaline texturing process (including saw-damage etching, texturing and surface cleaning) is performed for all groups prior to the diffusion processes. An atmospheric pressure (AP) $POCl_3$ diffusion process forms the homogeneous emitter for the reference groups as well as for the LoTSOx approach in Group A2. For the HiTSOx approach in Group B2, an adapted low pressure (LP) $POCl_3$ diffusion with only the deposition step is performed [6]. Laser diffusion from the phosphosilicate glass (PSG) forms the highly doped region of the selective emitter [8, 9] in Group B2. Then, for all groups, a chemical edge isolation process removes the emitter on the rear side, including the PSG removal on both sides. Subsequently, a wet chemical surface cleaning oxidizes a very shallow part of the emitter surface. The grown oxide is then removed in diluted hydrofluoric acid (HF) prior to the thermal oxidation processes. For the reference groups, a conventional low temperature oxidation process [2, 7] is used (one wafer per slot in vertical orientation), whereas for Group A2, a similar process is used but in this case with horizontally stacked wafers in an experimental setup, see Figure 3. For Group B2, an adapted high temperature stack oxidation is performed. Subsequently, the rear side of all groups is deposited with a passivation stack of $AlO_x/SiO_xN_y/SiN_z$ using plasma enhanced chemical vapor deposition (PECVD). For the front side, silicon nitride (SiN_x) is also deposited by PECVD, serving as anti-reflection coating and surface passivation. For Group A1/2 and B1, the "standard" SiN_x layer is used. For Group B2, a layer adapted in thickness is used to maintain low reflectance. After passivation, some samples (fabricated in a different batch) are fired and measured by quasi-steady-state photoconductance (QSSPC) to determine the implied open-circuit voltage iV_{oc}. For the cells, an infrared laser process locally removes the rear stack layers to form a dot-shaped local contact opening (LCO) for the remaining samples. The metallization is applied using screen-printing. For the rear side a full-area aluminum paste is used. The front side contains 120 fingers without busbars printed in a silver grid. After screen-printing, contact firing is performed in an industrial conveyor belt furnace with variation in the peak temperature. Then, the PERC cells are regenerated to mitigate boron-oxygen (BO) related light-induced degradation [10]. Finally, current-voltage measurements are performed in an industrial inline cell tester. For characterization, 1 cm-wide stripes are cut from selected solar cells to determine the specific contact resistance ρ_c for the front contact according to the transfer length measurement (TLM) [11].

Besides the PERC cell fabrication, symmetric lifetime samples are fabricated to investigate the emitter dark saturation current density j_{0e} of different combinations of diffusion and oxidation processes. Therefore, *n*-type Cz-Si wafers with a base resistivity of $\rho_b \approx 6\ \Omega$cm are used. After the texturing sequence, a variation in $POCl_3$ diffusion is performed (four different LP $POCl_3$ processes and the reference AP $POCl_3$ process). Then, the PSG is wet chemically etched on both sides. The surfaces are wet chemically cleaned. The thermal oxidation is varied using five different high temperature stack oxidations and the reference low temperature oxidation. The variations in diffusion and oxidation aim to cover a wide range of

<table>
<tr><th>Group A1 / B1</th><th>Group A2</th><th>Group B2</th></tr>
<tr><td colspan="3">p-type Cz-Si</td></tr>
<tr><td colspan="3">Texturing</td></tr>
<tr><td colspan="2">AP POCl$_3$ standard diffusion, $R_{sh} \approx 90\ \Omega$/sq</td><td>LP POCl$_3$ diffusion, $R_{sh} \approx 140\ \Omega$/sq</td></tr>
<tr><td colspan="2"></td><td>Laser doping, $R_{sh} \approx 80\ \Omega$/sq</td></tr>
<tr><td colspan="3">Chemical edge isolation + PSG etch</td></tr>
<tr><td colspan="3">Surface cleaning + HF cleaning</td></tr>
<tr><td>Low temperature conventional oxidation</td><td>Low temperature stack oxidation</td><td>High temperature stack oxidation</td></tr>
<tr><td colspan="3">PECVD passivation stack on rear</td></tr>
<tr><td colspan="2">PECVD SiN$_x$ capping on front „standard"</td><td>PECVD SiN$_x$ capping on front „adapted"</td></tr>
<tr><td colspan="3">Local laser contact opening on rear</td></tr>
<tr><td colspan="3">Aluminum screen printing on rear</td></tr>
<tr><td colspan="3">Silver screen printing on front</td></tr>
<tr><td colspan="3">Contact firing</td></tr>
<tr><td colspan="3">BO regeneration</td></tr>
<tr><td colspan="3">Current-voltage measurement, contact resistance measurement</td></tr>
</table>

Figure 2: Experiment plan for two solar cell batches A and B, whereby the reference groups A1 and B1 are fabricated similarly. Group A2 represents the low temperature stack oxidation approach (LoTSOx) and Group B2 the high temperature stack oxidation (HiTSOx) approach.

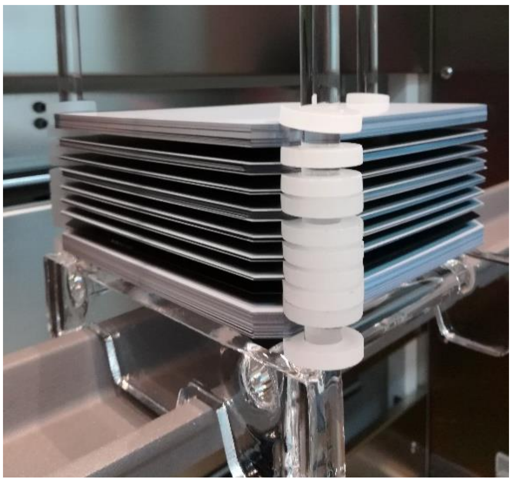

Figure 3: Experiment setup for stack oxidation processes. In this quartz boat, wafer groups can be separated by quartz rings.

emitter sheet resistances R_{sh} which is measured by means of inductive coupling [12]. Subsequently, both sides are passivated with either the standard SiN_x for the reference group or the adapted SiN_x for the HiTSOx approach applied by PECVD and the samples are fired. These symmetrical test samples are then characterized using QSSPC measurements to determine the effective lifetime at five spots per sample. Then, j_{0e} is obtained by the procedure described in Ref. [13].

4 RESULTS

4.1 LoTSOx

Table 1 shows the current-voltage characteristics for the LoTSOx approach (group A2 in Figure 2) and the reference process sequence (group A1 in Figure 2) measured in an industrial cell tester after BO regeneration. Comparing the median results of the measurement shows that the LoTSOx approach as well as the reference process sequence result in PERC solar cells with an energy conversion efficiency η of $\eta \approx 22.2\%$. The short-circuit current density j_{sc} and the open-circuit voltage V_{oc} are measured to be $j_{sc} \approx 40.4$ mA/cm^2 and $V_{oc} \approx 673$ mV, respectively, while the fill factor is about $FF \approx 81.7$ %. The best PERC cells in this investigation yield $\eta = 22.2\%$ for both process sequences. In the investigation in Ref. [5], we found that free-standing wafers in a thermal oxidation process show an about 3 nm thicker silicon dioxide in comparison to stacked wafers. Apparently, the different behavior of the silicon dioxide growth has no significant influence on the solar cell performance as the results are independent on the loading configuration that was used for the thermal oxidation process.

To summarize, the LoTSOx approach enables high throughput thermal oxidation processes without energy conversion efficiency losses due to stacking.

Table 1: Current-voltage characteristics of the PERC solar cells fabricated by LoTSOx approach (A2) as well as for the reference group (A1). The median and the best cell for each group are shown. The number of cells per group is shown in brackets. The measurements are performed by an industrial cell tester after boron-oxygen regeneration.

	Process sequence	j_{sc} / (mA/cm^2)	V_{oc} / mV	FF / %	η / %
Median	Ref (6)	40.4 ± 0.1	673 ± 1	81.7 ± 0.1	22.2 ± 0.1
	LoTSOx (4)	40.4 ± 0.1	673 ± 1	81.6 ± 0.1	22.2 ± 0.1
Best	Ref	40.4	673	81.7	22.2
	LoTSOx	40.4	674	81.7	22.2

4.2 HiTSOx

The emitter sheet resistance R_{sh} and the emitter dark saturation current density j_{0e} measured using the symmetric lifetime samples are shown in Figure 4 for the variation of LP $POCl_3$ diffusion processes and high temperature stack oxidation processes in the HiTSOx approach. This investigation shows j_{0e} between

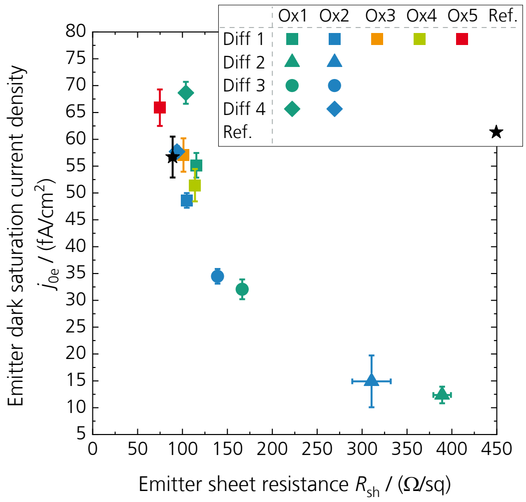

Figure 4: Emitter dark saturation current density j_{0e} on textured surfaces after SiO_2/SiN_x passivation and firing as a function of the emitter sheet resistance R_{sh}.

12 fA/cm^2 < j_{0e} < 69 fA/cm^2 within a wide range of emitter sheet resistance of 389 Ω/sq > R_{sh} > 73 Ω/sq. With stacking the wafers during high temperature oxidation, j_{0e} down to j_{0e} = (12 ± 2) fA/cm^2 at R_{sh} = (389 ± 10) Ω/sq is reached. For the combination of "Diff 4" and "Ox 2", R_{sh} and j_{0e} values similar to the ones for the reference manufacturing sequence (j_{0e} = (57 ± 4) fA/cm^2 at R_{sh} = (89 ± 4) Ω/sq) are achieved. Compared to the reference sequence, the combinations in the HiTSOx approach result in up to 15 nm thicker oxide thicknesses [5]. This is the reason why the SiN_x thickness needs to be somewhat thinner to maintain low reflectance at 600 nm wavelength. However, the different ratios between SiO_2 thickness and SiN_x thickness for the reference group and the HiTSOx combination Diff 4 and Ox 2 does not influence the passivation quality.

The combination of Diff 1 and Ox 1 with j_{0e} = (55 ± 2) fA/cm^2 at R_{sh} = (115 ± 1) Ω/sq is chosen for the PERC fabrication in Group B2 (compare Figure 2). By the laser doping process, 150 µm-wide finger structures are formed resulting in a local sheet resistance of $R_{sh} \approx 80$ Ω/sq. The energy conversion efficiency for these PERC cells as well as for the reference group (see Group B1 in Figure 2) are shown in Table 2 (as also reported in Ref. [6]). The cells of the reference process using AP $POCl_3$ diffusion for homogeneous emitter formation yield a peak energy conversion efficiency of $\eta = 22.2\%$, while the cells with the HiTSOx approach and selective emitter peak at $\eta = 22.0\%$. Comparing median results, the reference process reaches $\eta \approx 22.2\%$ with $V_{oc} \approx 675$ mV while the HiTSOx approach results in $\eta \approx 21.9\%$ with the main loss in V_{oc} ($V_{oc} \approx 670$ mV). As the implied open-circuit voltages iV_{oc} for the reference sequence and the HiTSOx approach are almost equal (fabricated in a different batch) with iV_{oc} = 682 mV and iV_{oc} = 681 mV, respectively, the recombination in the contact area with the dark saturation current density in the metallized area and the dark saturation current density in the laser-doped area may be the reason for the V_{oc} loss. This needs to be further investigated.

We also determined the specific contact resistance ρ_c of the front contacts of the cells fabricated with the HiTSOx approach with selective emitter via TLM measurements. Table 3 shows the results for three different set peak firing temperatures $T_{set,peak}$. We reach

Table 2: Current-voltage characteristics of PERC solar cells fabricated by HiTSOx approach as well as for the reference group. The median and the best cell for each group are shown. The number of cells is shown in brackets. The measurements are performed by an industrial cell tester after boron-oxygen regeneration.

	Process sequence	j_{sc} / (mA/cm^2)	V_{oc} / mV	*FF* / %	η / %
Median	Ref (4)	40.3 ± 0.1	675 ± 1	81.6 ± 0.1	22.2 ± 0.1
Median	HiTSOx (6)	40.2 ± 0.1	670 ± 1	81.1 ± 0.1	21.9 ± 0.1
Best	Ref	40.3	675	81.7	22.2
Best	HiTSOx	40.3	672	81.1	22.0

Table 3: Specific contact resistances ρ_c for the HiTSOx approach with selective emitter obtained by transfer length method (TLM) measurements on alkaline textured and phosphorus-doped surfaces after contact firing with the respective set peak firing temperatures $T_{set,peak}$ (SiO_2 and PECVD SiN_x passivation layer).

Set peak firing temperature $T_{set,peak}$ / °C	Specific contact resistance ρ_c / mΩcm^2
820	0.63 ± 0.45
840	0.61 ± 0.51
860	0.57 ± 0.50

low specific contact resistances around $\rho_c \approx 0.6$ mΩcm^2, almost independent from $T_{set,peak}$. The ρ_c in our investigation is as low as for the reference process reported in Ref. [7], which also points out the successful implementation of the new HiTSOx approach.

As higher efficiencies are expected with selective emitter in comparison to homogeneous emitter, more investigations are necessary. Therefore, variations in diffusion, oxidation and laser processing need to be performed on cell level with the HiTSOx approach. However, this first cell experiment shows the promising potential of this high throughput application.

5 SUMMARY AND CONCLUSION

In this work, we fabricated PERC solar cells with two approaches for thermal oxidation enabling processing of more than 5,000 wafers by stacking the wafers which means up to 3.1 times higher throughput. The first one is the low temperature stack oxidation (LoTSOx) approach. Here, the commonly used low temperature thermal oxidation process is performed in a tube furnace while the wafer are horizontally stacked in the quartz boat. The median energy conversion efficiency is not influenced due to stacking of the wafers and reaches $\eta = 22.2\%$ with homogeneous emitter, which is the same as for the reference group with vertically loaded wafers (one wafer per slot).

The second approach uses a shortened $POCl_3$ diffusion with only the deposition step and a subsequent high temperature stack oxidation. The shortened diffusion process enables an additional 1.8 times higher throughput Together with the increased throughput in the oxidation process, it reduces the cost of ownership by 41% compared to the state-of-the-art PERC processing. PERC solar cells with laser-doped selective emitter fabricated with the HiTSOx approach exhibit a peak energy conversion efficiency of $\eta = 22.0\%$ and a median of $\eta = 21.9\%$ which is already high in comparison to the reference sequence with homogeneous emitter and conventional moderate thermal oxidation. Further, the HiTSOx approach yields low specific contact resistances of the front contact around $\rho_c \approx 0.6$ mΩcm^2 independent from the set peak firing temperature.

A variation in the diffusion and stack oxidation processes for the HiTSOx approach allows a wide range of emitter sheet resistances R_{sh} to be covered. Emitter dark saturation current densities as low as j_{0e} = (12 ± 2) fA/cm^2 are reached at R_{sh} = (389 ± 10) Ω/sq.

Promising results are reached with our approaches with highly increased throughputs. Further work will investigate the HiTSOx approach with a wide variation in the laser processing as well as homogeneous emitter formation to further improve high throughput solar cell processing.

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