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KERFLESS WAFERING APPROACH WITH SI AND GE TEMPLATES FOR SI, GE AND III-V EPITAXY

Charlotte Weiss, Waldemar Schreiber, Marion Drießen, Ralf Sorgenfrei, Tingzhu Liu, Markus Ohnemus, Stefan Janz
Fraunhofer Institute for Solar Energy Systems ISE
Heidenhofstrasse 2, 79110 Freiburg, Germany

ABSTRACT: We work on the transfer from CZ wafers to epitaxially grown Si and Ge wafers on reusable substrates with a porous detachment layer ("kerfless wafering") to reduce material and energy consumption. We report on our progress of applying the kerfless wafering approach to Si and to Ge wafers. For Si, we develop templates and epitaxially grown wafers (SiEpiWafers) since many years in our self-made CVD reactor ("RTCVD") and are now bringing their quality to the next level with a new, microelectronic CVD reactor ("PEpi") which allows us to grow 6" and 156x156 mm² (M0) epitaxial Si wafers with adjustable thickness and doping level (*n*- and *p*-type). In the first test runs, we achieved as-grown lifetimes up to 840 µs and a total thickness variation of ~ 10%. For Ge, we were successful in developing and understanding a porous layer stack leading to 4" detachable Ge templates for future Ge or III-V epitaxial growth.
Keywords: Porous Silicon, Porous Germanium, Epitaxy, Lifetime

1 INTRODUCTION

For Si as well as for III-V solar cells, the wafer price is still a significant share (around 30% for Si) of the total costs [1]. Therefore, the transfer from CZ wafers to epitaxially grown Si and Ge wafers on reusable substrates with a porous detachment layer is an attractive approach ("kerfless wafering", Fig. 1) to reduce material and energy consumption. Kerfless wafering starts with Si or Ge seed wafers, which are porosified by electro-chemical etching. The subsequent annealing step leads to the reorganization of the porous layer, including the formation of a closed surface which acts as template for epitaxial growth and a highly porous lift-off layer underneath. For high epitaxially grown wafer quality, smooth, stress and defect free Si- and Ge-templates are necessary.

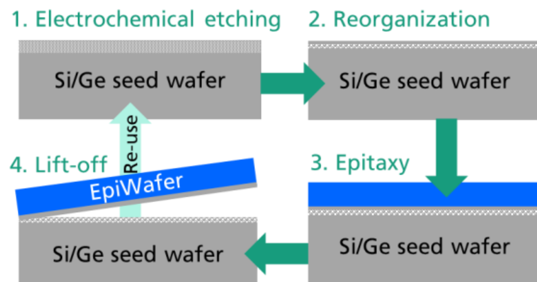

Fig. 1: Kerfless wafering scheme: 1. Porosification by electro-chemical etching of a c-Si/c-Ge wafer. 2. Reorganization process at high temperatures under H_2 3. Expitaxial Si, Ge or III-V growth. 4. After lift-off of the EpiWafer, the seed wafer can be re-used in the next cycle.

We have been developing processes for Si-templates and Si epitaxially grown wafers (SiEpiWafers) since many years in our self-made room temperature chemical vapor deposition ("RTCVD") reactor and high lifetimes are reported on unique samples [2]. However, process related quality limitations occur on many samples. A recent work showed that metal contamination limits the wafer quality and the reactor geometry leads to wafer bowing and artificial defects [3]. Therefore, a new atmospheric pressure CVD reactor ("PEpi") has been installed in our lab which allows the growth of high quality SiEpiWafers due to an extremely homogeneous temperature distribution (< 1 K) over the wafer, a significantly reduced introduction of contaminations into the process and an improved sample mounting. The first results from the PEpi reactor will be presented in this work.

Recently, we started to transfer our know-how of SiEpiWafers to Ge. The first results on porosification and reorganization are promising and will be presented in the second part of this contribution.

2 EXPERIMENTAL

2.1 Porosification

The electro-chemical process for etching of porous layers is quite different for Si and Ge substrates and therefore needs different setups.

The porous Si layers presented in this work are on 6", highly boron doped wafers, provided by IMS (Institut für Mikroelektronik Stuttgart, Fig. 3). They contain a porous layer stack of two highly porous layers under a lowly porous layer (Fig. 3a).

For the Ge porosification, highly Ga-doped ($\rho \approx 20$ mΩcm) 4" Ge [100] wafers with a miscut of 6° towards the [111] plane provided by UMICORE were used. Porous Ge layers were etched electrochemically in a batch tool provided by AMMT in HF electrolyte. Due to a different passivation behavior in comparison to Si, it is thus necessary to apply alternating current during the etching process [4,5].

2.2 Reorganization and Epitaxie

The Si reorganization step and the Si expitaxial growth are conducted in one of the two RTCVD reactors (RTCVD100 [6] (Fig. 2a) or RTCVD160 [7]) since many years and are transferred to a CVD batch reactor from LPE (PE 2061S "PEpi") at the moment (Fig. 2b). In both reactors, we use the same precursor gases for epitaxial growth ($SiHCl_3$ and H_2), for doping (Diborane (B_2H_6) and Phosphine (PH_3)) and for etch back (HCl). A reorganization time of several minutes was chosen in both reactors as well as a reorganization and epitaxy temperature $\geq$ 1090°C. The deposition rate in the old reactor is higher ($\approx$ 4 µm/min) than in the new reactor ($\approx$ 1 µm/min). However, the main differences between the RTCVD and the PEpi are the following: First, the sample holders in the RTCVD are made from quartz glass, whereas the sample holder in the PEpi (called susceptor) consists of SiC coated graphite.

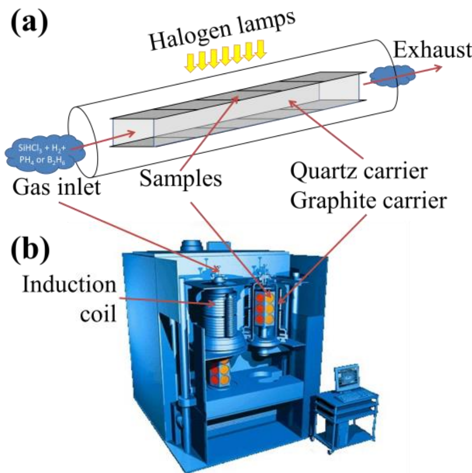

Fig. 2: Schematic of a) the RTCVD reactor chamber and b) the PE2061 reactor "PEpi" (new reactor).

The second important difference is the sample mounting. In the RTCVD, the samples are only locally supported by the samples carrier (Fig. 2a) and mounted horizontally. Therefore gravity can lead to bowing of the samples. In the PEpi, the samples are mounted vertically and are in full area contact with the susceptor (Fig. 2b). The third important difference is the optical heating (RTCVD) versus induction heating (PEpi). The induction heating allows for an extremely high thermal stability over the whole susceptor in the PEpi reactor. Another advantage of the PEpi is capability of change between 4" (18 samples per batch), 6" (12 samples per batch) and M0 (10 samples per batch) susceptors, whereas the RTCVD allows for 100x100 mm^2 samples maximum.
The wafer arrangement in the PEpi is as follows: The 4" wafers are lined up in 3 rows in the susceptor (Fig. 2b) whereas the 6" and M0 samples are arranged in two rows. The precursor gas inlet is located over the top row of the samples.

For Ge, only reorganization was done on 4" wafers in the RTCVD. The temperature used (700°C) was below the reorganization temperature of Si.

2.3 Preparation of lifetime samples

As no Ge epitaxy is established so far, we produced only lifetime samples from SiEpiWafers. Therefore, the wafers were cut with a chip saw in pieces up to 100x100 mm² after epitaxy and EpiWafers were detached manually with a self-made lift-off tool. The free standing SiEpiWafer are released from the remaining porous Si on the rear side by a KOH etch, followed by a RCA cleaning procedure and Al_2O_3 passivation on front and rear side. After a forming gas anneal, the lifetime samples are ready for measurements.

2.4 Characterization

To determine the structure of the porous Si and Ge layers before and after reorganisation, Secondary Electron Microscopy (SEM) was conducted at cross sections achieved by simple breaking. The roughness of the closed Ge template was measured by Atomic Force Microscopy (AFM). Thickness mapping of epitaxially grown Si was done with a laser interference tool by comparing the wafers thickness before and after epitaxy. Lifetime was measured by the Quasi Steady State Photoconductance (QSSPC) technique for an average value and by Photoluminescence spectroscopy (PL) for lifetime images. To determine the doping level of epitaxial Si, we used Spreading Resistance Profiling (SRP) and 4 point probe mappings (4pp) to investigate the homogeneity in depth and over the wafer area, respectively.

3 SILICON RESULTS

3.1 Porous Si (porSi) and Si reorganization (ReOrga)

For the first SiEpiWafer from the new PEpi reactor, we decided to use well-known templates. Therefore, we used 6" IMS porSi (Fig. 3a), described in the experimental section. The ReOrga of IMS porSi was studied in detail in the RTCVD reactors [3,8]. We know that during ReOrga, the two high porosity layers transform to a release layer whereas the low porosity layer closes to a smooth template, ready for epitaxy (Fig. 3b).

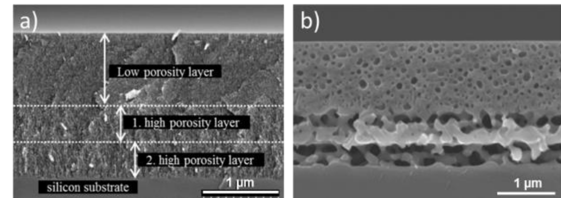

Fig. 3: SEM image of porous IMS sample a) before and b) after reorganization at 1120°C. A thick low-porosity layer on top of two high-porosity layers with slightly different porosities is clearly visible [3].

A typical ReOrga step in the RTCVD takes 2 min@1120°C. In the PEpi, we tried 5 min ReOrga in a temperature range from 1090°C…1120°C which led all to a successful lift-off of SiEpiWafers. For the first experiments, we focused on a high number of samples and therefore detached 40x50 mm² pieces. However, one run was dedicated to maximize the lift-off area and let to our first 100x100 mm² (pseudo-square) SiEpiWafer from a 6" seed wafer.

3.2 Epitaxially grown Si wafers

For the SiEpiWafer from the PEpi reactor, we aimed at a growth rate of 1 µm/min, a homogeneous thickness of ≈ 150 µm and a constant doping level (in depth and over the wafer area) of ≈ 1 Ωcm.

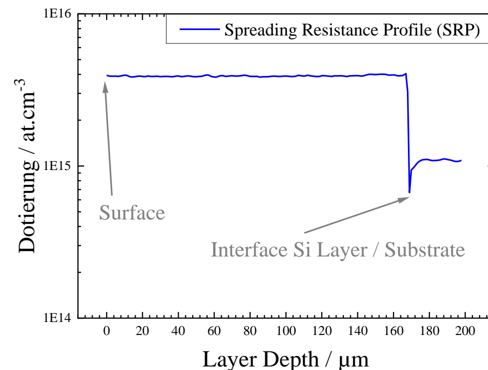

Fig. 4: Spreading resistance (SRP) depth profile of epitaxially grown Si layer in the PEpi reactor. The doping level is remarkably constant over the whole depth (from the layer surface until the interface to the substrate).

All this objectives were fulfilled during the first runs in the PEpi by adapting the precursor and doping gas flows as well as the temperature.

As an example, we show the doping level over the depth of the wafer in Fig. 4 and the thickness distribution from two runs (Run A und Run B) before and after adaption of process parameters (Fig. 5).
Fig. 4 shows the SRP profile without any adaption of the process. The doping is very homogeneous to $4x10^{15}$ at/cm³ (1.2 Ωcm) over the whole depth of the Si layer.

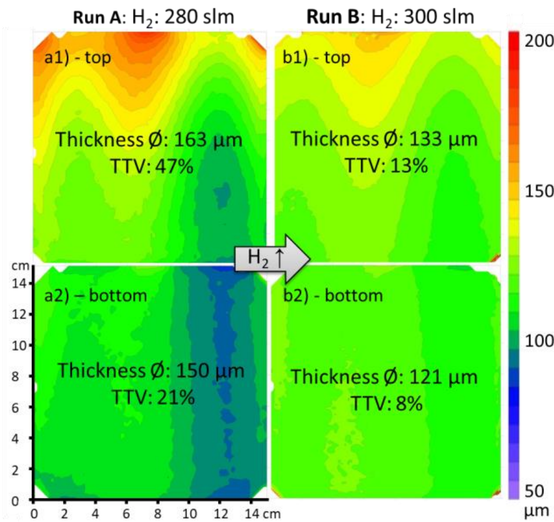

Fig. 5: Thickness mappings from two runs in the PEpi reactor. Respectively 2 samples from a top and a bottom position of the susceptor are shown. The thickness variation in Run A (a1 and a2) was reduced due to an increase in H_2 flow in Run B (b1 and b2). The thickness homogeneity is expressed by the total thickness variation (TTV).

During a deposition in the PEpi reactor, there are two rows of samples, a top and a bottom one. The precursor gas inlet is located over the top row of the samples. In Run A, a significant thickness gradient is observed with highest thickness on the upper part (Fig. 5a1) and lowest thickness on the lower part of the susceptor (Fig. 5a2). This means that near the gas inlet, the deposition rate is increased, probably due to a higher concentration of $SiHCl_3$ than in the lower part of the susceptor. The increase of the H_2 flow from 280 slm in Run A to 300 slm in Run B leads to a significant improvement of the thickness homogeneity. The top row sample is still thicker than the bottom row sample, but the total thickness variation (TTV) decreases from more than 20% in Run A to around 10% in Run B. We attribute this improvement to a more homogeneous TCS distribution over the whole susceptor due to the higher dilution in H_2. However, this leads to an unintended decrease of the growth rate from Run A to Run B (decrease of wafer thickness of ≈ 30 µm). This decrease in growth rate is tolerable in favor of the increase in thickness homogeneity at this time.

3.3 Quality limitations in SiEpiWafers

In recent years, we've put a lot of effort to understand the limitation of the quality of our SiEpiWafers from the RTCVD reactors. It is known that the most detrimental crystal defects are stacking faults with polycrystalline inclusions (polySF). Therefore, they were investigated carefully [9,10]. The characterization of single polySF by µPL, µRaman and SEM revealed the surrounding stress field, dislocations and that the polySF origins at oxide or other contaminations at the interface of template and Si epitaxy or local detachment [10]. To understand how the properties of the Si template influence the SiEpiWafer quality, a comprehensive study on the nature of the porSi before and after reorganization (AFM, Reciprocal Space Maps) was done [3]. A deformation of the crystal lattice during reorganization was observed and explained. However, both studies showed that in the end, the quality is limited mostly by an overall background contamination with transition metals, thermal stress due to temperature inhomogeneity and wafer bowing due to gravity during the process. This is demonstrated by the PL lifetime mapping in Fig. 6a. There, the presence of slip lines, dislocations and stacking faults cannot explain the overall low lifetime of ≈ 20 µs [3].

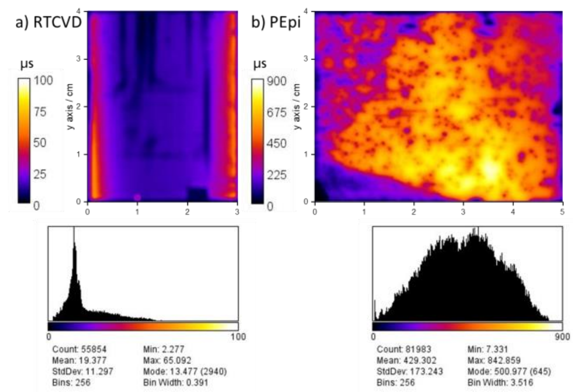

Fig. 6: As-grown PL lifetime image of SiEpiWafer from a) RTCVD and from b) new, microelectronic CVD reactor (PEpi) taken at 1 sun.

The influence of the background contamination was tested recently by annealing experiments of reference Si FZ wafers (*p*- and *n*-type) in the RTCVD at 900°C for 30 min under H_2 (Fig. 7). For wafers with SiC diffusion barriers between wafer rear side and quartz sample holder, the lifetimes increase by one order of magnitude indicating a contamination from the quartz carriers. The big difference between Si *n*- and *p*-type further confirms the influence of contamination.

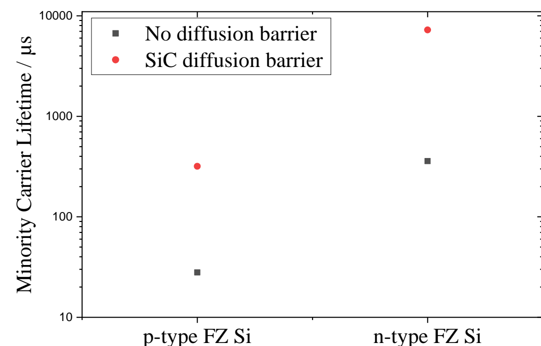

Fig 7: Effect of back side diffusion barrier on the lifetime of reference FZ samples annealed in the RTCVD for 30 min at 900°C.

In the new CVD reactor, the contamination from the sample holder is avoided by the use of SiC-coated graphite instead of quartz. Additionally, the sample holder is coated with polySi before every epitaxy run. The susceptor in the PEpi allows for a vertical, fully supported sample mounting instead of horizontal, locally supported samples mounting the RTCVD. Also the thermal homogeneity is much better due to inductive instead of optical heating. This resulted in a significant increase in lifetime already for the SiEpiWafers from the first PEpi runs. The lifetime image of the best 40x50 mm² piece on IMS porSi for now is shown in Fig. 5b) with a mean value of 420 µs and maximum values > 800 µs. As these values are as-grown (without gettering step) and without parameter optimization to reduce defects, we expect to reach a multiple of these first lifetime values in the near future.
As mentioned before, in the old reactors, the expenditure for generation a smooth, stress free Si template during ReOrga has never been able to pay off in good lifetime results due to the high background contamination. With the new reactor and our experience in terms of template optimization, we now have the tool to study the interaction between template and epi properties in detail.

We get a first impression of this kind of analysis by looking at Fig. 5b) again. The dark spots in the middle of the sample (bad lifetime spots) correlate with SFs on the sample. We also tried to grow Si in the PEpi directly on polished Cz Si wafers (without porous layer) and know that this leads to nearly SF free Si layers. Therefore, we conclude that the SF in Fig. 5b) are template related. Possible reasons could be for example open pores, oxygen residuals, roughness etc. This will be examined in much more detail soon.

4 GERMANIUM RESULTS

4.1 Porous Ge

With the bipolar etching process, there is the possibility to realize several types of porous Ge structures [4]. The parameters influencing the structure are, among others, the pulse duration and current density ratios. The successfully prepared sponge like layer is shown in Fig. 8a).

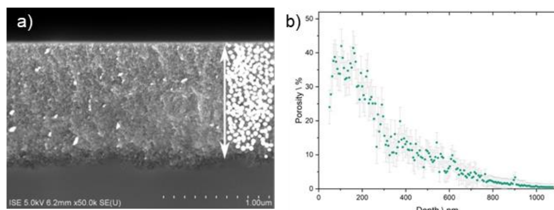

Fig. 8: a) Bipolar electrochemically etched sponge-like layer. b) Porosity in dependence of depth for the porous layer showed in a) gained by focused ion beam milling (FIB).

The main goal was the generation of a porosity gradient throughout the whole layer depth. This creates a continuous transition from the porous layer to solid. In a subsequent annealing step, this favours the diffusion of atoms to the layers with a lower porosity and finally results in a separation layer. By using the focussed ion beam milling (FIB) method on this structure, it was possible to calculate the porosity in dependence of depth (Fig. 8b) by determining the ratio between bulk and void of each SEM image. This clearly shows the change in porosity although using constant etching parameters.

4.3 Ge reorganization (ReOrga)

The combination of different types of layers enables the possibility to create different porous layer stacks. Especially a less porous layer above the sponge layer fulfils the requirement of a closed top layer after annealing. Due to the higher porosity of the separation layer and it's porosity gradient, Ge-atoms move during the annealing step to the low porous top and to the low porous interface porous layer/bulk. The reorganization leads to a fully closed top layer followed by a separation layer mostly consisting of voids (see Fig. 9a). The surface of the reorganized template is measured by AFM (Fig. 9b) and shows a RMS of ≈ 5 nm. This value predicts a successful III-V epitaxial growth.

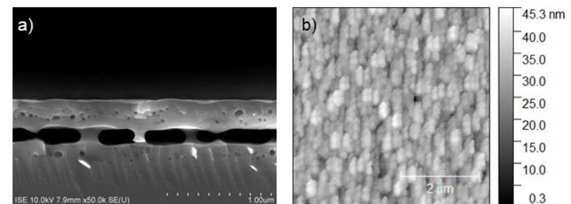

Fig. 9: a) Annealed structure with clearly closed top layer followed by a separation layer mainly consisting of voids and connection points between the Ge bulk and the top layer designated as breaking points. b) AFM image of the surface showed in e) with a RMS value of ≈ 5 nm.

The combination of several types of porous Ge structures enables a wide range of possibilities to vary the thickness of the top layer and separation layer. Investigations on crystal quality will be done by XRD in the future to investigate the template quality further.

5 CONCLUSION

5.1 Silicon

For the fabrication of SiEpiWafer with the kerfless wafering approach, we referred to well-known porous layers, allowing us to focus on Si epitaxy in our new reactor "PEpi" and compare the results with our reactor "RTCVD". We show the successful growth of Si epitaxy on 6" and M0 wafers with adjustable layer thicknesses around 150 µm and adjustable doping level around 1 Ωcm with the precursor gases $SiHCl_3$, H_2 and PH_3. With a H_2 flow of 300 slm, we reach a good total thickness variation of ≈ 10%. We successfully lifted-off SiEpiWafers with a maximum area of 100x100 mm² (pseudo-square). The best average lifetime of 430 µs was measured on a 40x50 mm² SiEpiWafer with locally 840 µs, which can be improved by improving the reorganization step as well as by applying a gettering step.

We showed that our dominant lifetime limitation in the RTCVD reactor was induced stress due to temperature gradient, sample mounting and transient metal contamination from the quartz sample holder. Using a SiC coated graphite carrier for vertical sample mounting in the new reactor instead of a quartz carrier is successfully tackling all these issues. The new reactor will allow the correlation between template

characteristics and epitaxy quality in the near future.

5.2 Germanium

For Ge, we found an approach to understand the formation of different porous layers and their combination in stacks. We were successful in etching and reorganizing a porous Ge stack on a 4” wafer. A fully closed Ge template upon a detachment layer could be achieved. FIB-REM measurement allow for a determination of the porositiy change in depth which will further help us to understand and improve the template.

The Ge templates open several routes for epitaxy. The first one is the growth and lift-off of epitaxial Ge (GeEpiWafers). This will be possible in the new reactor by applying $GeCl_4$. The second route is the direct growth of III-V layers on the Ge template in the MOVPE reactor at our institute and the comparison with III-V layers grown on Ge bulk. The latter is an ongoing experiment.

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