

HIGH THROUGHPUT LOW ENERGY INDUSTRIAL EMITTER DIFFUSION AND OXIDATION

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ABSTRACT: In this work, we investigate an approach of shortened low pressure (LP) POCl_3 diffusion and a high throughput thermal oxidation with stacked wafers to form the emitter for passivated emitter and rear cells (PERC). As the high temperature processes such as LP- POCl_3 diffusion and thermal oxidation account for a significant share of the manufacturing costs of PERC solar cells, our high throughput approach is very promising in terms of reducing both, production costs and energy consumption. Compared to state-of-the-art POCl_3 diffusion and low temperature oxidation, a 40% reduction of the specific costs and a 50% reduction of the energy consumption of the high temperature processes is feasible. We examine this approach by using four different adapted LP- POCl_3 diffusion processes using only the deposition phase (omitting further drive-in and in-situ oxidation) in combination with a “stack oxidation” process. Detailed characterization of the properties of the emitter and oxide layers after diffusion and after oxidation confirm a high quality emitter formation resulting in emitter dark saturation current density $j_{0e} \approx 32 \text{ fA/cm}^2$ at $R_{sh} \approx 183 \text{ } \Omega/\text{sq}$. Although the wafers are oxidized in a stack of horizontally oriented wafers touching each neighboring wafer, a very homogeneous oxide grows resulting in high passivation quality. Further, we find that this adapted emitter diffusion process allows for effective laser doping, which is promising for selective emitter formation.

Keywords: High throughput, wafer stacks, LP- POCl_3 diffusion, thermal oxidation, laser doping, silicon oxide

1 INTRODUCTION

The passivated emitter and rear cells (PERC) structure [1] gained a significant world market share in the last decade and will remain the mainstream technology in industry in the next years [2]. The process sequence for PERC solar cells usually contains two high temperature processes: A tube furnace diffusion using phosphorus oxychloride (POCl_3) as liquid dopant source is the most common technology to form the emitter [2] and a thermal oxidation or anneal (also in a tube furnace) mostly serves as emitter passivation [3]. A cost of ownership (COO) analysis [4] shows, that these two processes account for a share of 11% of the PERC cell production costs. Energy conversion efficiencies η close to 22.5% are currently achieved for PERC solar cells with homogeneous emitters [5–7] using Czochalski-grown silicon (Cz-Si) wafers. In order to further increase η , the selective emitter has come back into focus in recent years [7–12] and its market share will increase significantly [2]. The selective emitter can be formed by, e.g., local laser doping from the phosphosilicate glass layer [13]. In order to further reduce the production costs of solar cells, a huge increase of the production tool throughput is predicted from 8000 wafers per hour in 2020 to 12000 wafers per hour in 2030 [2]. One option to realize a higher throughput is to increase the density of wafers per process by stacking the wafers during diffusion [14] or oxidation [15].

This work investigates an approach to reduce the specific costs and the energy consumption of the high temperature processes by decreasing the process time of the low pressure (LP) POCl_3 diffusion and by increasing the throughput during thermal oxidation. Hence, this study investigates the combination of shortened LP- POCl_3 diffusion processes applying only the deposition phase (omitting the drive-in phase) and a high throughput oxidation by stacking the wafers. We study the achievable charge carrier concentration profiles, the emitter recombination properties, the oxide growth, and

the combination with laser doping in comparison to a reference state-of-the-art high temperature process route.

2 STATE-OF-THE-ART EMITTER FORMATION

The state-of-the-art emitter formation technique for PERC cells is the tube furnace diffusion using POCl_3 as liquid dopant source. This POCl_3 diffusion often includes a deposition phase and a subsequent drive-in phase usually at elevated temperatures, as depicted in Figure 1. The deposition phase takes place on a first temperature plateau with nitrogen (N_2) flow through the POCl_3 bubbler. Further, oxygen (O_2) gas flow is also active. The ratio between N_2 - POCl_3 and O_2 is moderate at this step, where the phosphosilicate glass / silicon dioxide (PSG/SiO_2) layer [16, 17] grows on the surface of the wafer (during this step, a moderate in-diffusion of phosphorus in the wafer takes also place), acting as a

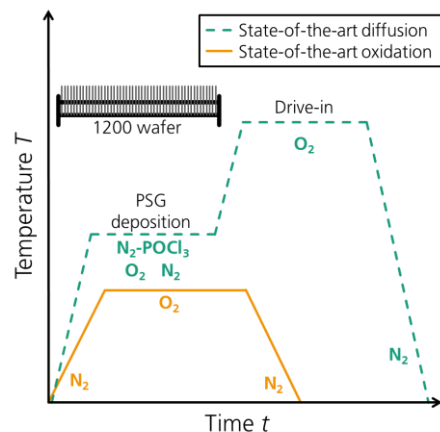


Figure 1: Schematic illustration of the state-of-the-art tube furnace diffusion and oxidation processes as a function of the temperature T over time t . Throughput of both processes: 1200 wafer.

donant source in the subsequent drive-in phase. There, a high O₂ gas flow is often introduced to the process tube [8, 18, 19]. For this so-called in-situ oxidation the furnace is usually ramped up to temperatures above 850°C [20–22]. The goal of the in-situ oxidation is to decouple the phosphorus source from the silicon (Si) surface and thus to control or reduce phosphorus (P) in-diffusion from this source. Due to the increased throughput, the POCl₃ diffusion at low pressure (LP) [23] dominates in production. The LP-POCl₃ diffusion is typically performed in a horizontal quartz boat with vertical wafer arrangement and a typical wafer pitch of 2.38 mm with a throughput of 1200 wafers per run.

For boosting the efficiency of PERC solar cells, a selective emitter can be implemented on the front side of the PERC solar cell [7–12]. The approach often used for the realization of the selective emitter formation is laser doping from the PSG/SiO₂ layer.

Emitter passivation for PERC cells mostly involves a thermal oxidation or annealing process [3]. Figure 1 depicts the course of a state-of-the-art thermal oxidation process. It features moderate temperatures [3, 6, 7] well below those of the diffusion process and it is also performed in a tube furnace similar to the diffusion process. During this process, gaseous N₂ and O₂ are used [24–26]. During oxidation in the O₂ atmosphere a layer of silicon dioxide grows into the silicon surface. This layer serves as a surface passivation – in particular in combination with hydrogen rich capping layers. Such low temperature thermal oxidation processes do hardly affect the doping profile [6].

3 APPROACH

The approach investigated in this paper applies an adapted LP-POCl₃ diffusion in combination with a high throughput oxidation by stacking wafers.

We adapt the LP-POCl₃ diffusion process by reducing the process to its PSG/SiO₂ layer deposition step, as depicted in Figure 2. In this step, only the PSG/SiO₂ deposition and a moderate in-diffusion of phosphorus take place. No drive-in or in-situ oxidation at elevated temperature is performed since the thermal treatment required for the further in-diffusion of phosphorus is transferred to the subsequent thermal

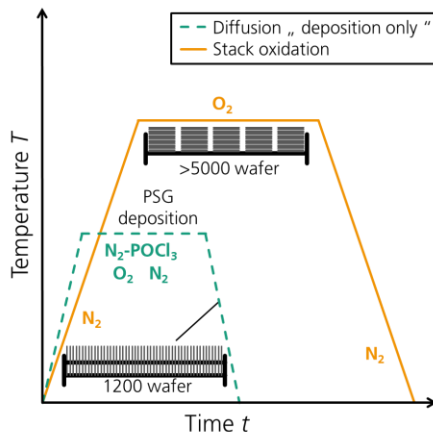


Figure 2: Schematic illustration of the approach in this work: Adapted tube furnace LP-POCl₃ diffusion and the high throughput thermal oxidation using wafer stacks (>5000 wafer).

oxidation process. This significantly reduces the process time for the LP-POCl₃ diffusion step compared to the state-of-the-art diffusion, keeping the typical load of 1200 wafers per process.

During the thermal oxidation process in this work, the wafers are stacked horizontally on top of each other with their surfaces touching each other. Thus, the throughput may be significantly increased to more than 5000 wafers per run, as depicted in Figure 2. However, this high throughput oxidation process features a higher temperature and longer process time compared to the state-of-the-art process. Stack diffusion [14] and stack oxidation [15] processes have been proposed and industrially applied earlier. The high throughput thermal oxidation process with stacked wafers is simply referred to as “stack oxidation” below.

The PERC solar cell fabrication sequence for our approach with selective emitter would be analogous to the state-of-the-art sequence, only the diffusion and thermal oxidation processes are adapted.

4 COST CALCULATION

We calculate the cost of ownership (COO) for our state-of-the-art process route for PERC solar cells with LP-POCl₃ diffusion and low temperature thermal oxidation, as well as for the novel approach proposed in this paper. The calculations were conducted with the “SCost” COO model [4], which is aligned to the SEMI standards E35 [27] and E10 [28]. The model input data is based on industrial equipment and process parameters. The results are depicted in cost split charts in Figure 3. For this calculation the wafer throughputs mentioned in section 3 are assumed. By shortening the LP-POCl₃ process, the COO for this process reduces from 1.50 €/ct/Wafer to 0.94 €/ct/Wafer (same amount of 1200 wafer per process). Comparing the thermal oxidation processes, the state-of-the-art low temperature thermal oxidation features a shorter process time and a lower thermal budget than the high throughput thermal oxidation, but the latter has a much higher load with 5000 wafers per process assumed here. This results in a 3.2 times higher throughput for the stack oxidation. Also taken into account is the increased investment cost for the

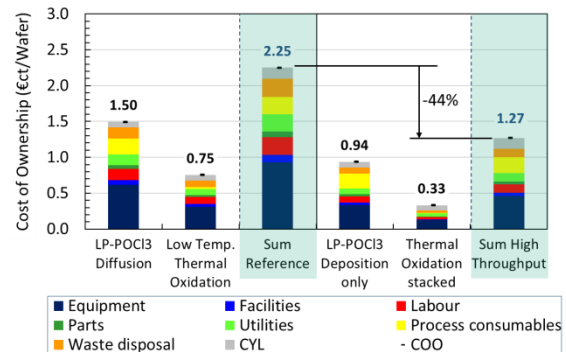


Figure 3: Cost of ownership (COO) calculation for the state-of-the-art process route with LP-POCl₃ diffusion (1st bar) and low temperature thermal oxidation (2nd bar), as well as for the approach presented in this paper with LP-POCl₃ only deposition diffusion (4th bar) and thermal oxidation using stacked wafers (5th bar). The sum of the COO for the state-of-the-art process route is stated in the 3rd bar and for the new approach in the 6th bar.

equipment which is assumed to be 30% higher for the high throughput thermal oxidation tool due to adapted automation and increased mechanical strength of the paddle which is necessary for the higher load. Nevertheless, the COO reduces from 0.75 €/Wafer for the low temperature oxidation to 0.33 €/Wafer for the stack oxidation. In total, the COO for both thermal processes reduces from 2.25 €/Wafer for the state-of-the-art processing to 1.27 €/Wafer with the presented approach. This is a reduction of the COO by 44%. For the specific power consumption, taking into account the heat capacity of the Si wafers, a reduction of approximately 50% is expected due to reduced heat losses.

5 EXPERIMENT

In this investigation, four groups of test samples are manufactured, depicted in Figure 4, for the characterization of the PSG/SiO₂ and thermal oxide growth (group 1), of the sheet resistance R_{sh} and charge carrier concentration profiles before and after oxidation (group 2), of laser doping (group 3) and of the passivation quality (group 4). Therefore, M2 p-type and n-type Cz-Si wafers serve as starting material for group 1 to 3 and group 4, respectively. Either a saw damage etch (SDE) or alkaline texturing is performed for group 1 or for groups 2 to 4, respectively, before four different LP-POCl₃ diffusion processes only with deposition step (see section 5.1) form the emitter and the stack layer system of PSG/SiO₂.

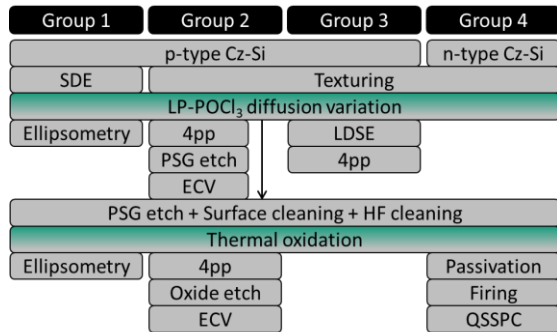


Figure 4: Experiment plan for the test samples investigated in this work.

For group 1, we perform ellipsometry measurements using a laser ellipsometer after the LP-POCl₃ diffusion to measure the layer thickness of the PSG/SiO₂ layer stack that forms during the POCl₃ deposition. The ellipsometry measurement consists of 25 measurement points distributed over the wafer surface, assuming a refractive index of 1.5 as proposed in Ref. [17].

Some test samples of group 2 are characterized by means of the four-point-probe (4pp) technique to determine the sheet resistance R_{sh} . For the determination of the charge carrier concentration profiles, the electrochemical capacitance-voltage (ECV) measurement [29] is used after PSG etching to yield the charge carrier concentration as a function of the depth. The surface area factor is adjusted such that the R_{sh} calculated from charge carrier concentration profile matches the R_{sh} measured with 4pp close to the ECV measurement spot [30, 31].

The test samples of group 3 are partly laser-doped

(full area test fields, 1x1 cm²) using a green ns laser (532 nm wavelength) and three different laser parameter sets “P1” to “P3” with increasing laser pulse energy $E_p = \{47 \mu\text{J}; 52 \mu\text{J}; 62 \mu\text{J}\}$. Some areas on the wafer remain untreated by the laser and serve as reference. The test samples are also characterized by 4pp to determine R_{sh} after laser doping.

The following PSG/SiO₂ etch in hydrofluoric acid (HF) removes the dopant source for groups 1, 3 and 4, and the remaining wafers in group 2. Then, for all groups, a wet chemical cleaning step oxidizes a very shallow part of the highly doped emitter surface. The grown oxide is then removed again in diluted hydrofluoric acid (HF) prior to the thermal oxidation process where the wafers are stacked on top of each other (see section 5.2).

For group 1, ellipsometry measurements are repeated after thermal oxidation to determine the SiO₂ layer thickness using the same procedure as described above. For group 2, 4pp measurements determine R_{sh} after thermal oxidation. Subsequently, the grown SiO₂ is etched before the charge carrier concentration profiles are determined using ECV.

Group 4 is further processed by depositing a silicon nitride SiN_x on both sides using plasma enhanced chemical vapour deposition (PECVD). Subsequent to the following fast firing step for the activation of the hydrogen passivation, these symmetrical test samples are characterized using a quasi-steady-state photo conductance (QSSPC) measurement to determine the effective lifetime at five different spots per sample. Then, the emitter dark saturation current density j_{0e} is obtained by the procedure described in Ref. [32].

5.1 LP-POCl₃ diffusion

Table 1 shows process parameters of the PSG/SiO₂ deposition step for the reference process “Ref” and for the processes “Dep. T1” to “Dep. T4” investigated in this work. Our diffusion processes are developed in a LP-POCl₃ tube furnace from centrotherm international AG. The reference process “Ref” features a deposition temperature of $T_{dep} = 800^\circ\text{C}$ (deposition temperatures are set temperatures in the tube furnace) while the gas flow ratio between N₂-POCl₃ and O₂ is 0.26. This reference process benefits from a subsequent in-situ oxidation at elevated temperature and a second deposition phase at deposition temperature $T_{dep,2} > T_{dep}$ to increase the amount of phosphorus within the PSG layer [16, 17]. The target of the variation in the novel LP-POCl₃ diffusion processes “Dep. T1” to “Dep. T4” is to have a sufficient high reservoir of phosphorus atoms incorporated in the silicon wafer as well as in the PSG layer immediately after the deposition step. This is beneficial for the further in-diffusion of the phosphorus atoms during the following laser doping process as well as for their redistribution during the subsequent thermal oxidation process. Therefore, we increased the N₂-POCl₃/O₂ ratio

Process	Temperature $T / ^\circ\text{C}$	N ₂ -POCl ₃ /O ₂ ratio
Ref	800	0.26
Dep. T1	805	0.80
Dep. T2	800	0.80
Dep. T3	798	0.80
Dep. T4	795	0.80

Table 1: Process parameters during PSG/SiO₂ deposition step of the LP-POCl₃ diffusion processes (see also Figure 2 for the process flow).

compared to the reference process to 0.8. We varied the deposition temperature of the PSG/SiO₂ deposition processes, decreasing from $T_{\text{dep}} = 805^\circ\text{C}$ for “Dep. T1” to $T_{\text{dep}} = 795^\circ\text{C}$ for “Dep. T4”.

5.2 Thermal oxidation

In combination with the reference diffusion process “Ref”, described in section 5.1, a reference thermal oxidation featuring moderate temperature is used. In this low temperature thermal oxidation the wafers are vertically orientated in a conventional quartz boat. The adapted diffusion processes “Dep. T1” to “Dep. T4” are combined with a high throughput thermal oxidation process that is conducted within an industrial tube furnace also from centrotherm international AG. A special quartz boat is used as depicted in Figure 5. Here, the wafers are stacked horizontally on top of each other. This quartz boat uses the common paddle for automated loading and unloading of the process chamber. The wafers are loaded manually to the quartz boat, but automatization of this wafer loading process is conceivable. With quartz rings, it is possible to separate groups of wafers in this quartz boat. Free standing horizontal samples separated using these quartz rings serve as reference samples.



Figure 5: Experimental set-up for the stack oxidation process using a horizontal industrial tube furnace. Different groups of horizontally stacked wafers in this quartz boat are separated by quartz rings.

The process flow of the oxidation is as follows (see also Figure 2): The process atmosphere inside the tube is exchanged right after loading by evacuating and subsequent filling with nitrogen (N₂). The temperature is ramped up in N₂ to the plateau temperature. When reaching the plateau temperature, the atmosphere switches to pure oxygen (O₂) by using the vacuum pump. Before cool-down, the atmosphere is again changed to N₂.

6 RESULTS

6.1 LP-POCl₃ diffusion processes

Figure 7 shows the sheet resistance R_{sh} and the PSG/SiO₂ layer thickness d_{PSG} for the diffusion processes characterized as described in chapter 5. The sheet resistance R_{sh} of the reference process “Ref” is found to be $R_{\text{sh}} = (105 \pm 6) \Omega/\text{sq}$. For diffusion process “Dep. T1”

(highest $T_{\text{dep}} = 805^\circ\text{C}$), the sheet resistance is $R_{\text{sh}} = (137 \pm 3) \Omega/\text{sq}$ and increases to $R_{\text{sh}} = (167 \pm 3) \Omega/\text{sq}$ with decreasing $T_{\text{dep}} = 795^\circ\text{C}$ for “Dep. T4”. Further, the reference process features a thick PSG/SiO₂ with $d_{\text{PSG}} = (40 \pm 1) \text{nm}$. In contrast, increasing T_{dep} and omitting the subsequent heat-up and the in-situ oxidation after the deposition step for the processes “Dep. T1” to “Dep. T4” reduces d_{PSG} significantly to $(24 \pm 1) \text{nm} < d_{\text{PSG}} < (27 \pm 1) \text{nm}$. The reduction of T_{dep} from process “Dep. T1” to process “Dep. T4” affects the PSG/SiO₂ thickness only slightly.

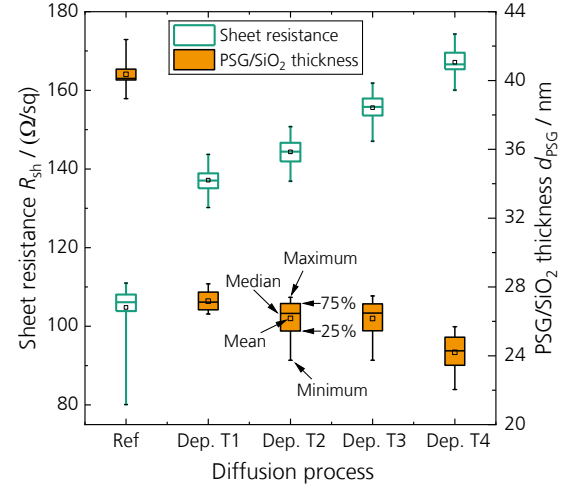


Figure 7: Sheet resistance R_{sh} (4pp with PSG/SiO₂ layer on textured surfaces, 100 measurement points) and PSG/SiO₂ thickness d_{PSG} (ellipsometry on SDE surfaces, 25 measurement points) for the different diffusion processes.

Figure 6 shows a selection of the ECV measurements. For reasons of clarity, only the charge carrier concentration profiles of diffusion “Dep. T1” and “Dep. T4” are shown. The R_{sh} values given in the graph are higher than the ones obtained in Figure 7 as R_{sh} is measured in the wafer center after PSG etching in Figure 6 while in Figure 7, it is measured over the whole wafer surface before PSG etching. The charge carrier concentration profiles show a surface concentration N_s of

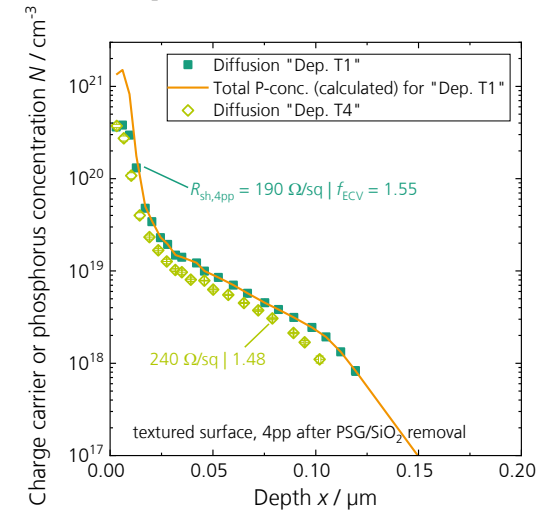


Figure 6: Charge carrier concentration profiles obtained by ECV technique after PSG/SiO₂ etch on textured surface in the wafer center, scaled to locally measured R_{sh} . Further, the total phosphorus concentration calculated from the ECV profile according to Ref.[33].

$N_s \approx 4 \cdot 10^{20} \text{ cm}^{-3}$ for both processes. The profile depth x_d extracted at a concentration $N = 1 \cdot 10^{17} \text{ cm}^{-3}$ is found to be $x_d \approx 150 \text{ nm}$ for process “Dep. T1” and slightly less for “Dep. T4”. According to Ref. [33], we calculate the expected total amount of phosphorus from the electrically active phosphorus concentration determined with ECV (also shown in Figure 6). The difference between the predicted total phosphorus concentration profile and the measured charge carrier concentration profile gives the share of electrically inactive phosphorus. At the surface and in the surface near region, this difference in the concentration is quite high. The expected total phosphorus surface concentration $N_{s,\text{total}}$ increases significantly by about a factor three to $N_{s,\text{total}} = 1.5 \cdot 10^{21} \text{ cm}^{-3}$ compared to the surface concentration from ECV. The high amount of electrically inactive phosphorus will be activated in the following thermal oxidation step, which will be discussed in section 6.3.

6.2 Laser doping processes

In this section, we investigate the performance of diffusion process “Dep. T1” in comparison to the reference process “Ref” regarding the change in sheet resistance R_{sh} by laser doping. Figure 8 shows the R_{sh} measured for the laser-doped test fields (applying the laser parameter set “P1”–“P3”) and for the test fields without laser doping (“no”). For the reference diffusion “Ref”, R_{sh} decreases from $R_{sh} \approx 107 \text{ } \Omega/\text{sq}$ without laser processing down to $R_{sh} \approx 70 \text{ } \Omega/\text{sq}$ when applying laser parameter set “P3” with the highest pulse energy. In contrast, the PSG/SiO₂ deposition process “Dep. T1” starts at $R_{sh} \approx 130 \text{ } \Omega/\text{sq}$ without laser processing and R_{sh} reduces down to $R_{sh} \approx 21 \text{ } \Omega/\text{sq}$ when laser parameter set “P3” is applied. The combination of low power laser parameter set “P1” with the PSG/SiO₂ deposition process “Dep. T1” results in $R_{sh} \approx 53 \text{ } \Omega/\text{sq}$, which is still lower than $R_{sh} \approx 67 \text{ } \Omega/\text{sq}$ reached by the reference diffusion “Ref” applying a higher laser power “P3”. Starting with a higher R_{sh} (without laser doping) for diffusion “Dep. T1” compared to the reference process, a lower R_{sh} is reached with the same laser parameter set in comparison to the reference process. A reason for this could be the thinner PSG/SiO₂ layer for “Dep. T1” compared to “Ref” (see Figure 7). Lohmüller et. al. [16] showed that a diffusion process with only performing a deposition step features a

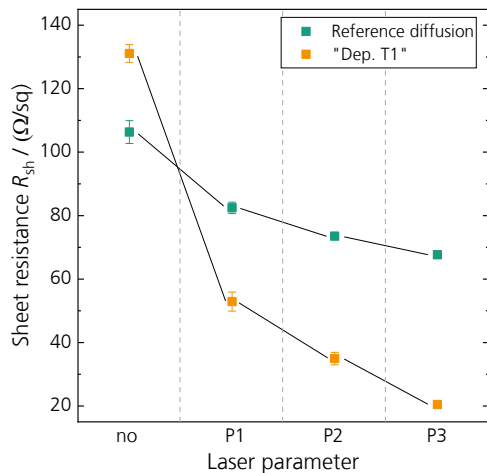


Figure 8: Sheet resistance R_{sh} for two diffusion processes (“Reference” and diffusion process “Dep. T1”) after laser doping with parameters “P1” – “P3” and without laser doping “no”. The solid lines serve as a guide to the eye.

thin intermediate SiO₂ layer. Their work showed that thinner intermediate oxide layers correlate with enhanced R_{sh} reduction by laser doping [34]. Further, the activation of already incorporated electrically inactive phosphorus [35], see again Figure 6, could be a reason for the more effective doping observed in this work.

6.3 Thermal oxidation processes

This section discusses the results of the characterization of the thermal oxidation process. Figure 9 depicts the sheet resistances R_{sh} after the thermal oxidation processes. Here, the reference diffusion “Ref” with $R_{sh} = (105 \pm 6) \text{ } \Omega/\text{sq}$ is combined with the reference low temperature thermal oxidation which slightly increases R_{sh} to $R_{sh} = (118 \pm 5) \text{ } \Omega/\text{sq}$. For the PSG/SiO₂ deposition processes “Dep. T1” to “Dep. T4” in combination with the stack oxidation, the R_{sh} increases constantly with decreasing diffusion temperature, as expected. Interestingly, the stack oxidation decreases R_{sh} for diffusion “Dep. T1” (highest T_{dep}) by $\Delta R_{sh} \approx 7 \text{ } \Omega/\text{sq}$ to $R_{sh} = (130 \pm 2) \text{ } \Omega/\text{sq}$. In contrast to that, the stack oxidation process clearly increases R_{sh} for the deposition processes with lower T_{dep} , especially “Dep. T4”. Here, an increase of $\Delta R_{sh} \approx 18 \text{ } \Omega/\text{sq}$ to $R_{sh} = (185 \pm 4) \text{ } \Omega/\text{sq}$ is observable after the stack oxidation process.

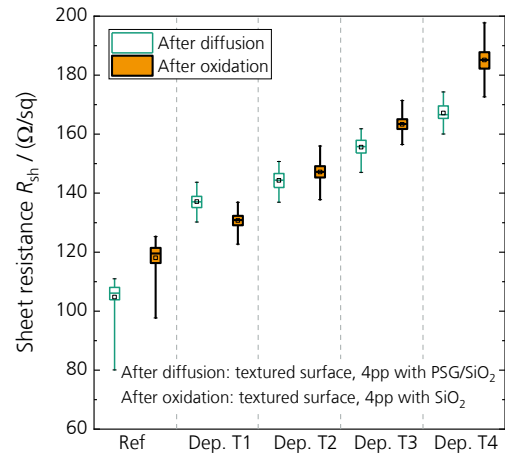


Figure 9: Sheet resistance R_{sh} after diffusion and thermal oxidation process, measured with 4pp (100 measurement points over the wafer).

Figure 10 shows selected charge carrier concentration profiles for the different diffusion processes after the thermal oxidation processes. For diffusion “Dep. T1”, the profile after diffusion from Figure 6 is also included. The reference sequence with diffusion “Ref” and low temperature oxidation results in a surface concentration $N_s \approx 1.5 \cdot 10^{20} \text{ cm}^{-3}$ and a depth of $x_d \approx 250 \text{ nm}$. For “Dep. T1”, the surface concentration decreases from $N_s \approx 4 \cdot 10^{20} \text{ cm}^{-3}$ after diffusion to $N_s \approx 1.5 \cdot 10^{20} \text{ cm}^{-3}$ after the stack oxidation, while the depth increases to $x_d \approx 200 \text{ nm}$. The profile for the combination of the adapted LP-POCl₃ diffusion “Dep. T1” only with deposition step and the stack oxidation is very similar to the one of the reference process. From “Dep. T1” to “Dep. T4” after stack oxidation, the surface concentration decreases slightly, as well as the depth of the charge carrier concentration profiles. Calculating the total amount of phosphorus for “Dep. T1” after the stack oxidation according to Ref. [33], shows that the oxidation significantly reduces the expected total phosphorus

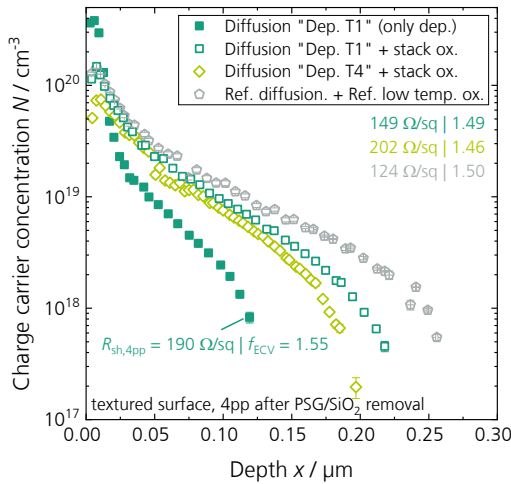


Figure 10: Charge carrier concentration profile obtained by ECV technique after SiO₂ etch on textured surface. Filled green squares represent the doping profile already depicted in Figure 6. The empty symbols show the doping profiles after the stack oxidation.

concentration at the surface to $N_{s,total} \approx 2 \cdot 10^{20} \text{ cm}^{-3}$ (not shown here), which is only slightly higher than the active charge carrier concentration (compare Figure 10).

The respective oxide layer thicknesses d_{Ox} grown on the silicon surfaces during the thermal oxidation processes are measured using ellipsometry and depicted in Figure 11. The reference diffusion with the low temperature thermal oxidation yields an oxide thickness of $d_{Ox} \approx 4 \text{ nm}$ with excellent homogeneity over the wafer and over the process boat. In contrast, the stacked oxidation yields much thicker layers, partly due to the higher oxidation temperature. Additionally to the wafers oxidized as a stack, single free-standing wafers in horizontal position are investigated. The oxide thickness of the free-standing samples decreases constantly from $d_{Ox} = (21.5 \pm 0.6) \text{ nm}$ for “Dep. T1” to $d_{Ox} = (18.2 \pm 0.7) \text{ nm}$ for “Dep. T4”. The oxide growth depends on the phosphorus concentration at the surface N_s [36, 37]: The higher the concentration, the higher the oxide growth rate. “Dep. T1” shows the highest surface concentration (compare Figure 10), which leads to the thickest oxide (see Figure 11). The surface concentration decreases with decreasing deposition temperature from

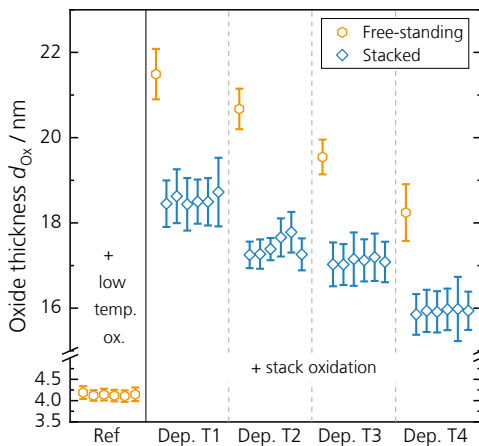


Figure 11: Silicon oxide layer thicknesses on SDE surface measured with ellipsometry (25 measurement points over the wafer) after diffusion and thermal oxidation.

“Dep. T1” to “Dep. T4” (see Figure 10) and so does the oxide thickness (see Figure 11). Furthermore, d_{Ox} decreases as well for the stacked samples from $d_{Ox} \approx 18 \text{ nm}$ for “Dep. T1”, over $d_{Ox} \approx 17 \text{ nm}$ for “Dep. T2” and “Dep. T3” to $d_{Ox} \approx 16 \text{ nm}$ for “Dep. T4”. The oxide thickness is only about 2 to 3 nm lower for wafers oxidized as stack compared to the free standing ones. Thus, the availability of O₂ within the gap between the stacked wafers is sufficient to grow a uniform oxide layer. The homogeneity over the wafer is excellent with standard deviations below 1 nm as well as the homogeneity over the stack with a standard deviation of about 0.5 nm.

6.4 Emitter recombination

Figure 12 shows the emitter dark saturation current density j_{0e} as a function of the sheet resistance R_{sh} for the reference process with state-of-the-art diffusion and low temperature thermal oxidation as well as for free-standing and stacked samples with adapted diffusion and stack oxidation. It has to be mentioned that all samples were coated with a SiN_x layer of similar thickness, although the underlying oxide layer is of different thickness (compare Figure 11). The reference process results in $j_{0e} = (50 \pm 3) \text{ fA/cm}^2$ at $R_{sh} = (115 \pm 2) \text{ Ω/sq}$. The j_{0e} for the high throughput approach decreases with increasing R_{sh} and decreasing N_s . For free-standing samples j_{0e} decreases continuously from $j_{0e} = (55 \pm 4) \text{ fA/cm}^2$ at $R_{sh} = (122 \pm 3) \text{ Ω/sq}$ for diffusion “Dep. T1” to $j_{0e} = (35 \pm 2) \text{ fA/cm}^2$ at $R_{sh} = (183 \pm 6) \text{ Ω/sq}$ for diffusion “Dep. T4”. A similar behavior is visible for the stacked samples, where j_{0e} decreases from $j_{0e} = (49 \pm 1) \text{ fA/cm}^2$ at $R_{sh} = (130 \pm 4) \text{ Ω/sq}$ for diffusion “Dep. T1” to $j_{0e} = (32 \pm 1) \text{ fA/cm}^2$ at $R_{sh} = (183 \pm 5) \text{ Ω/sq}$ for diffusion “Dep. T4”. Comparing stacked and free standing samples, j_{0e} is higher for the free standing samples, but R_{sh} is lower at the same time, thus no specific impact of the stacking on j_{0e} is observed. The low j_{0e} values achieved for the high throughput approach with adapted LP-POCl₃ diffusion (featuring only the deposition step) and stack oxidation suggests that the amount of highly recombinative electrically inactive phosphorus after the PSG/SiO₂ deposition process seems to be effectively reduced during the thermal oxidation process, as predicted using the model from Ref. [33] (see above).

To conclude, with the approach investigated in this work similar emitter properties can be achieved as for the

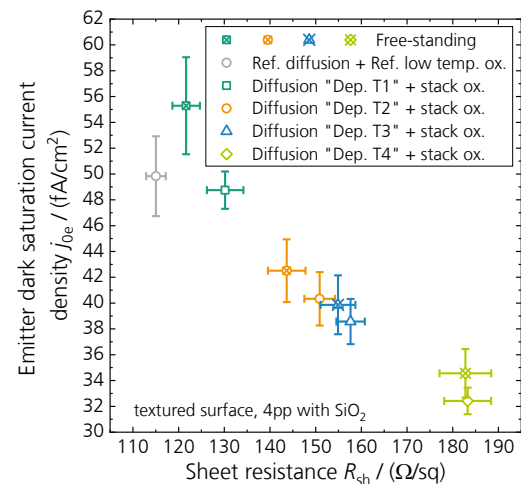


Figure 12: Emitter dark saturation current density for free-standing and stacked test samples.

state-of-the-art approach. However, the contacting of these emitters using screen-printed silver pastes and the integration into the PERC cell process needs to be proven additionally.

7 SUMMARY AND CONCLUSION

Shortening the process time of the LP-POCl₃ diffusion by omitting any drive-in step as well as increasing the throughput during thermal oxidation from 1200 to more than 5000 wafers per process by stacking the wafers, results in a reduction of the specific costs by 44%. Furthermore, the specific power consumption is reduced by approximately 50%.

The charge carrier concentration profile of our high throughput approach is very similar to the one of a state-of-the-art LP-POCl₃ diffusion with low temperature oxidation, which features a surface concentration of about 10²⁰ cm⁻³ and a profile depth in the range of 200 nm to 250 nm. The electrically inactive phosphorus available after the deposition step of the adapted LP-POCl₃ diffusion is reduced significantly due to the subsequent stack oxidation process. This is confirmed by yielding high-quality phosphorus emitters with emitter dark saturation current density j_{0e} values on textured surface between $j_{0e} \approx 50$ fA/cm² (SiO₂/SiN_x passivated and fired) at emitter sheet resistance $R_{sh} \approx 130$ Ω/sq and $j_{0e} \approx 35$ fA/cm² at $R_{sh} \approx 180$ Ω/sq for the high throughput approach. The results also show that stacking of wafers during thermal oxidation yields similar values for j_{0e} compared to free standing wafers.

The low j_{0e} values achieved for the high throughput approach also suggest that a thermal oxide with high passivation quality is grown on the wafer surfaces within the stack. The thickness of this oxide is found to be 16 nm < d_{Ox} ≤ 19 nm with an excellent homogeneity (standard deviation of 1 nm).

Implementing a laser doping process between diffusion and oxidation for realizing selective emitters shows that a more effective doping is possible for the adapted LP-POCl₃ diffusion process that features only the deposition step, than for the reference LP-POCl₃ diffusion process.

In summary, this high throughput approach with short LP-POCl₃ diffusion and stack oxidation is very promising for passivated emitter and rear cells processing featuring homogeneous as well as selective emitters.

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