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ENHANCED MATERIAL QUALITY IN SMART MONO-SI BLOCK CAST INGOTS BY INTRODUCTION OF FUNCTIONAL DEFECTS

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ABSTRACT: The use of cast-mono technology to control the development of structural defects during the block casting process enables the crystallization of Silicon for solar cells with good material quality at high throughput and low cost. The obstacles, ingrowth of parasitic grains and development of dislocation clusters, might be overcome by the SMART seeding technique, i.e. the introduction of functional defects. Ingots with the cast-mono and SMART seeding configuration, as well as a new approach including a monocrystalline spacer have been crystallized. Whereas the ingrowth of parasitic grains was reproduced with the standard cast-mono technique, the functional defects suppressed the ingrowth of parasitic grains until an ingot height of approx. 80 mm. By the introduction of an additional monocrystalline spacer, the ingrowth of parasitic grains could be avoided for the whole ingot height of 210 mm. The spreading of dislocation clusters in the monocrystalline area could be reduced significantly using the SMART approach in contrast to the standard cast-mono configuration. This reduction of structural defects enabled high bulk lifetimes above 1 ms on large wafer areas for both p- and n-type material after typical high efficiency solar cell processing steps.
Keywords: Crystallisation, Cast-Mono, Structural Defects, Lifetime

1 INTRODUCTION

With the evolution of the PERC structure [1] as the dominant solar cell technology in the market [2], the need for high quality silicon wafers as base material has substantially increased. This has led to the massive capacity extension of monocrystalline silicon wafers grown by the Czochralski method in the last years.

In contrast, the market share of multicrystalline wafers from block casting processes such as High Performance Multicrystalline Silicon (HP mc-Si) [3] is in sharp decline. Although high solar cell efficiencies of up to 22.3 % have been demonstrated on HP mc-Si with low dislocation densities, the characteristic grain boundaries as inherent crystal defects significantly limit the electronic quality of the wafer [4]. Impurities introduced by the crucible system during the growth process interact with grain boundaries and dislocations and enhance the electronic recombination activity of those structural defects.

The limitations by the multicrystalline structure of block cast processes can partly be overcome by the use of monocrystalline seed material leading to “cast-mono” (alternatively named as “quasi-mono” or “mono-like”) silicon wafers [5]. Whereas the introduction of this technology into main industrial production has failed in the past, a renewed interest in cast-mono (cm) processes and solar cells can be observed. The main obstacles for cast-mono growth processes are the unwanted ingrowth of parasitic grains from the crucible into the ingot volume and the introduction of dislocations originating mainly at the seed joints.

The SMART technology for cast-mono silicon ingots using functional defects for blocking parasitic grains as well as reducing dislocation generation has been introduced and proven on small scale [6, 7]. This work focuses on the implementation of the SMART technology in laboratory cast-mono growth processes of G2 sized ingots and its applicability into industrial processes. Combinations of differently oriented large seed plates with a stack of thin seed plates according to the SMART technique have been evaluated under the aspect of blocking parasitic grains nucleated at the crucible and preventing dislocation generation at the seed joints. The effect of the seeding configuration on the electronic material quality with respect to the use in high efficient solar cell processing has been investigated on passivated wafer level.

2 EXPERIMENTAL PROCEDURE

2.1 Ingot growth process

For this work, several G2 sized ingots have been produced in a laboratory Vertical Gradient Freeze (VGF) furnace. For all experiments, pre-coated G2 sized crucibles from Vesuvius (*SOLAR® Crucible HPC*^{TM}) have been used. Prior to crystallization, no pre-heating or modification of the crucible side or bottom structure has been done. Thus, the crucible system has been identical to the used setup for the growth of HP mc-Si and did not feature special adaptions for processing of cast-mono Si such as flattened crucible bottom or changed heat conductivity. About 65 kg of high quality Si feedstock were filled on top of a 30 mm high seed layer at the crucible bottom.

The size distribution of the feedstock was kept similar for all investigations. The thermal process consisted of a heating and melting phase of about 15 h and a crystallization phase with an average growth velocity of 7.5 mm / h followed by a rather long cooling phase of about 21 h. Doping was provided by use of highly Boron or Phosphorus doped silicon chips thus resulting in either p-type or n-type Si ingots. The thermal process was a “half-melt” process meaning that the thermal field in the melting phase was controlled such that the feedstock was molten from top down to the seed layer without completely melting the seeding material. The melt-growth interphase was kept flat to slightly convex with respect to the grown crystal. In all cases a height of 22 - 26 mm of the initial seed material was preserved.

2.2 Seed layer configuration

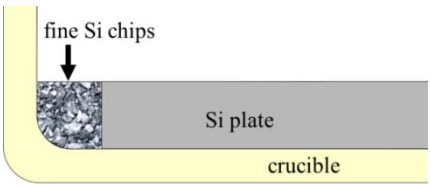
For all experiments, a seed layer consisting of predominantly monocrystalline Si material was placed on the crucible bottom prior to filling with polysilicon feedstock on top of the seed. Large monocrystalline plates (marked as "Si plate") with a <100> orientation in growth direction and a <110> orientation of the faces were used as seeds for the monocrystalline regions. Variations of up to 5 small monocrystalline silicon plates of 1 mm thickness corresponding to the length of the edge of the large seed plates were combined as a SMART stack according to the proposed technology [6, 7]. Small sized polysilicon feedstock in form of fine chips with a diameter smaller than 15 mm was used at the rim of the seeding layer which had a height of 30 mm over the whole area prior to melting.

In order to investigate the effect of the introduction of SMART stacks in comparison to the formerly dominating cast-mono process, several combinations of large seed plates with and without SMART stacks have been realized. The main aspects for the experiments were the ability for blocking parasitic grains nucleated at the crucible wall and reducing dislocation generation at the seed joints in the inner part of the ingot.

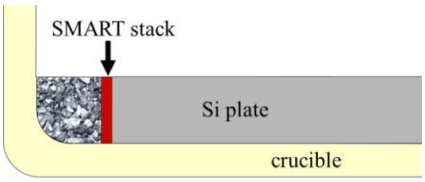
2.2.1 Blocking of parasitic grains at ingot edge

Three different seeding scenarios have been realized with seed combinations near the crucible wall. In order to reproduce the cast-mono process as originally introduced, a large Si plate was combined with fine Si chips in the gap between the plate and the inner crucible wall, configuration "cm" (see Figure 1(a)). In the second experiment, a SMART stack was placed in between the fine chips and the Si plate, configuration "SMART" (see Figure 1(b)) to block parasitic grains.

(a) Configuration "cm"



(b) Configuration "SMART"



(c) Configuration „mod. SMART"

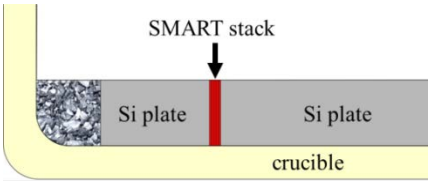


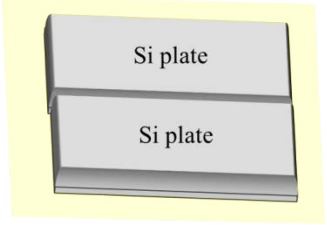
Figure 1: Investigated seeding scenarios for ingot region near crucible. View as cross section from the side.

The evaluation of these two experiments as discussed in paragraph 3 showed evidence that a third option could result in even better performance. For this the configuration "SMART" was revised by introducing a second Si plate of smaller lateral dimensions as a monocrystalline spacer, configuration "modified SMART" (see Figure 1(c)).

2.2.2 Reduction of dislocations at seed joints

For the use of advanced seeding in industrial processes, the seed configuration must be transferable to large ingot sizes such as e.g. G8. In order to reduce stress within the ingot, the SMART concept utilizes the functional defects as buffer between the large seed plates. Therefore, two different seeding configurations for the inner ingot region are compared. The first configuration "cm" represented the reference process with the large seed plates of the same crystallographic orientation touching each other. As new configuration "SMART" the SMART stack was placed in between the seed plates as shown in Figure 2.

(a) Configuration "cm"



(b) Configuration "SMART"

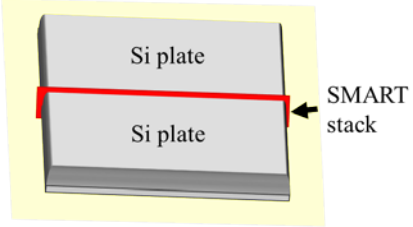


Figure 2: Investigated seeding scenarios for the inner ingot region.

2.3 Sample processing

Silicon bricks of 125 mm side length were cut from central and edge positions of the ingot and subsequently wafered to 190 µm thick wafers by diamond wire sawing. Additional vertical cuts from the edge region were processed for brick characterization.

For electrical material characterization, n-type and p-type wafers were selected from the middle and upper ingot heights. The n-type wafers received a damage etch and the high temperature processes of a high-efficiency TOPCon cell processing, i.e. BBr3 diffusion at 875 °C followed by an oxidation at 900 °C and a $POCl_3$ diffusion at 800 °C. After etch back of the diffused layers, the wafers were surface passivated by a 70 nm thick SiN_x layer.

The p-type wafers received after an alkaline etch a high temperature process as used for PERC cells, i.e. a $POCl_3$ diffusion at 860 °C. After emitter etch back, the wafers were passivated with a 20 nm thin Al_2O_3 layer on both sides with subsequent annealing at 400° for 10 min.

2.4 Characterization methods

The ingots were analyzed by optical and electrical inspection. Photoluminescence Imaging [8, 9]was used to

depict the minority carrier distribution from polished brick sides. It has to be noted that for these brick measurements the resistivity distribution has not been accounted for and thus, the PL images of brick samples do not show a calibrated lifetime distribution. Injection dependent lifetime on passivated wafers was measured by QSSPC and modulated PL [10, 11], the lifetime values were extracted at an injection level of $\Delta n \sim 10^{15}$ cm^{-3}.

3 RESULTS AND DISCUSSION

3.1 Material improvement by SMART seeding

In order to evaluate the changes in the material properties by the introduction of SMART stacks, the results of the growth experiments for seeding configurations “cm” and “SMART” are compared and discussed.

3.1.1 Blocking of parasitic grains

Seed configurations “cm” and “SMART” showed distinctly different crystal properties regarding the parasitic multicrystalline grains which grew from the small size Si chips at the seed border or nucleated at the crucible walls in all crystallization experiments.

Figure 3 depicts a photograph (left) and a PL image (right) of a cross section of the crystal structure from seeding configuration “cm”. The photo shows that directly at the bottom of the crucible wall, multicrystalline grains form and start overgrowing the monocrystalline bulk volume. This corresponds to the observation that for a flat or slightly convex growth interface parasitic grains usually overgrow the monocrystalline parts. Other approaches (e.g. [12, 13]) try to avoid nucleation and ingrowth by a highly convex growth interphase. This concept can force the grains back towards the ingot border. Specific growth process conditions such as the thermal field defined by a side heating system or travelling magnetic fields can suppress the ingrowth of grains substantially. However, such processes can lead to high thermal stress and thus the occurrence of significant dislocation clusters which massively impair the material quality.

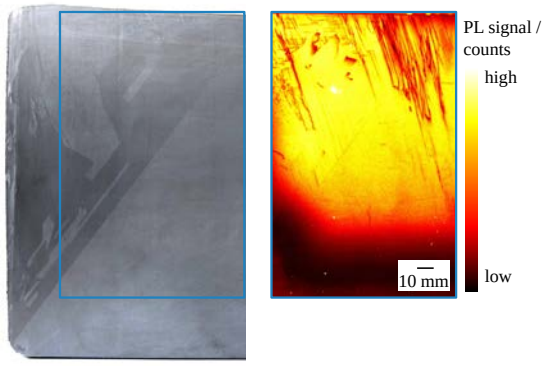


Figure 3: Photo (left) and PL image (right) corresponding to the indicated square of a cross section of an edge ingot with seed configuration “cm”. The crucible contact side was on the left hand side.

In the upper ingot region, a high density of structural defects evolves as can be seen in the PL image. These defects significantly reduce the material quality of the produced wafer with respect to solar cell processing.

By introducing the SMART stack near the crucible border between the fine Si material and the large monocrystalline seed plate, configuration “SMART”, the unhindered ingrowth of grains into the bulk volume can be diminished in the bottom region (see Figure 4 (left)). All grains with different orientation seem to be blocked by the perpendicular to the growth interface propagating grain boundaries induced by the SMART stack up to a height of approx. 80 mm.

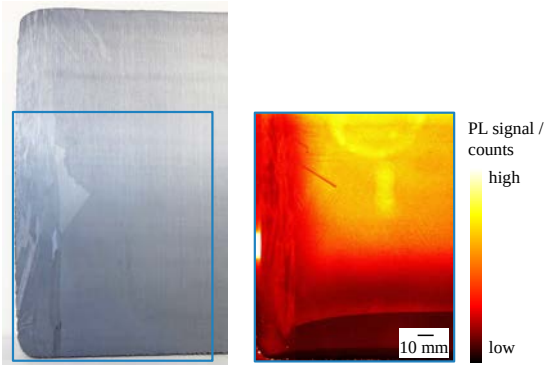


Figure 4: Photo (left) and PL image (right) corresponding to the indicated square of a cross section of an edge ingot with seed configuration “SMART”. The yellow round structure in the PL image is due to a measurement artefact.

However, it can be observed that above that critical height the initially straight grain boundary running parallel to the border of the monocrystalline plate changes its form. The stability of the grain boundary seems to be gradually modified with more parasitic grains coming into contact. Finally grains can overcome this barrier and grow into the mono region as can be seen at middle sample height (see Figure 4). In particular, this approach seems to be prone to the ingrowth of twin grains higher up in the ingot. This can induce the formation of dislocation tangles in the monocrystalline regions (see also section 3.1.2).

The corresponding PL image (see Figure 4 (right)) is dominated by a combination of the aforementioned crystal defects and the zone of reduced lifetime near the seed and the crucible border due to impurities. In the monocrystalline region on the right side of the functional defect region, the lifetime reduction is dominated by impurities coming from the crucible system. Only few recombination active structural defects can be found in that region in the bottom half of the ingot. A reduction of the indiffusion of impurities from the crucible could not be observed for the analyzed samples.

3.1.2 Dislocation development at seed joints

When using the “classical” seed configuration “cm” for the inner ingot region with two seed plates of the same orientation touching each other, a line of dislocation tangles can evolve directly above the seed joint (see Figure 5). With increasing height, shown here for 50 mm, 100 mm, and 150 mm, the dislocation clusters enlarge and form loops which diminish the material quality significantly. Especially in industrial processes using that seed configuration, the material quality of wafers from the top part of cast-mono ingots often was significantly reduced by a high area fraction of dislocation clusters [14–16].

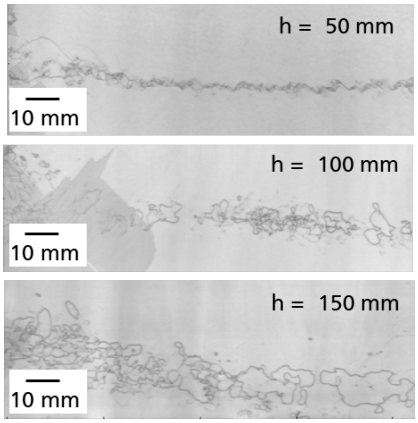


Figure 5: Photoluminescence images of the same crystal region above one seed joint of identically oriented seeds as in configuration "cm" for the inner ingot region measured on as-cut wafers from 50 mm, 100 mm, and 150 mm ingot height.

The formation of functional defects including large angle grain boundaries at the joint of different seeds within the ingot has been proposed for the minimization of dislocation clusters within the mono-like region. A possible solution to this is the SMART approach. When introducing a SMART stack between these seed plates (as in configuration "SMART" for the inner ingot region), two parallel large angle grain boundaries evolve which grow perpendicular to the growth interphase from seed region to the ingot top (see Figure 6). In between these parallel boundaries, dislocation tangles and small angle grain boundaries, visible as transverse line structures, form throughout the ingot height.

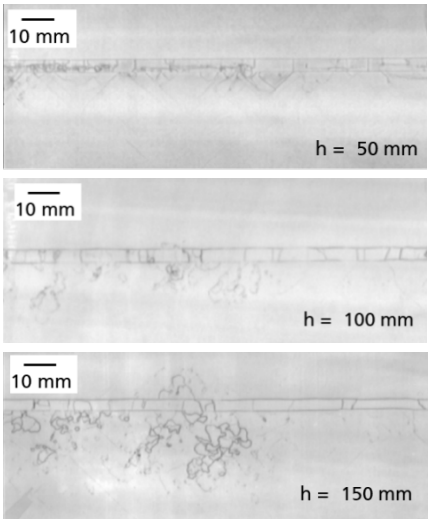


Figure 6: Photoluminescence images of the crystal region above a seed joint of identically oriented seeds including a SMART stack as in configuration "SMART" for the inner ingot region measured on as-cut wafers from 50 mm, 100 mm, and 150 mm ingot height.

Dislocation clusters within the monocrystalline regions form in the vicinity of the large angle boundaries starting already in the lower ingot region. In contrast to case "cm", up to about half the ingot height these dislocations do not form closed loops but stay in contact with the induced grain boundary. For regions higher in the ingot, these dislocations seem to decouple from the grain boundary and multiply as in case "cm". The overall wafer area impaired by the dislocations is significantly smaller for the SMART approach than for the classical seeding.

3.1.3 Electrical properties of wafers

In order to assess the material quality from these configurations with respect to its use in solar cell processes, selected wafers have been processed and analyzed as described in paragraph 2.3. Figure 7 shows the results for two n-type wafers from a cast-mono seeding on the left side and from a SMART mono seeding on the right side. Both wafers are from 175 mm ingot height and show corresponding wafer areas of 100 x 100 mm^2 with a distance of approx. 25 mm to the induced SMART functional defects for the right wafer.

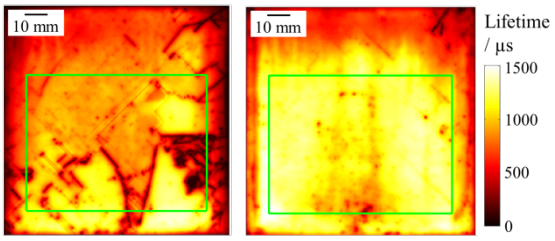


Figure 7: PL lifetime images of n-type passivated wafers after high temperature processing at an illumination corresponding to ~ 0.05 suns. The left wafer originates from an ingot with cast-mono seeding, the right wafer from SMART seeding.

The main difference in these images is the amount of strongly recombination active structural defects. Whereas in the left image a very high contrast between the dark line structures at the right edge and the adjacent grain yellow color coding can be observed, the amount of such strongly active structures is significantly reduced for the right wafer. The square-root harmonically averaged lifetime within the green frame corresponds to ~0.8 ms at $\Delta n = 7 \times 10^{14}$ cm^{-3} for the cast-mono wafer and ~1.2 ms at $\Delta n = 1 \times 10^{15}$ cm^{-3} for the SMART wafer. The wafer area outside this frame is affected by wafer-processing related lifetime reductions and, thus, not considered in the comparison. Both wafers have an n-type base resistivity of $\rho = 0.9$ Ωcm. Considering the difference in the lifetime values and the structure of recombination active defects, application of the SMART technique shows a promising improvement of material quality with respect to the cast-mono approach. Thus, the investigated material is suitable for high efficient solar cell structures such as the TOPCon approach.

3.2 Modified SMART seeding

The experiments with the SMART seeding configuration at the ingot edge have revealed an instability of the induced large angle grain boundaries resulting in the overgrowth of parasitic grains above a certain height. For all wafers from above that height the material quality is impaired by the ingrown grains and the corresponding structural defects. Depending on the growth interface near the crucible wall, this overgrowth can start early in the solidification process. A decrease of the number of grains interacting with the functional defect area should increase the chance of blocking all

grains from growing into the monocrystalline ingot region.

In order to decrease the number of parasitic grains interacting with the induced large angle grain boundaries, a small monocrystalline seed plate was introduced between the small sized chip material and the SMART stack as a spacer material. Using this modified SMART seeding configuration "mod. SMART" in conjunction with a slightly adapted thermal process, a p-type ingot with a grain structure as shown in Figure 9 was produced.

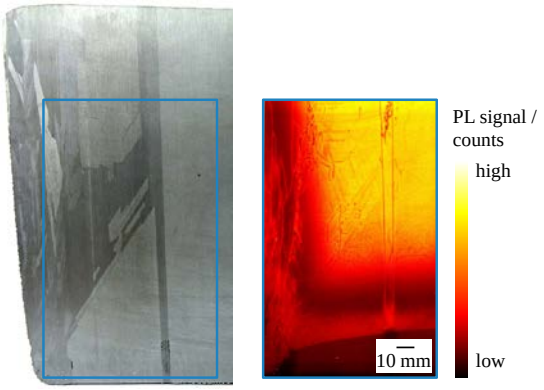


Figure 8: Photo (left) and PL image (right) corresponding to the indicated square of a cross section of an edge ingot with seed configuration "mod. SMART".

At lower ingot height, multicrystalline grains growing from either the small sized feedstock or the crucible are hindered to grow into the mono region by the thermal process for about 10 mm only. From about 40 mm upwards, various grains overgrow that barrier into the ingot volume. For the investigated samples, the ingrowing grains at a distance from the ingot edge larger than 35 mm were predominantly twins. Thus, the vertically formed large angle grain boundary induced by the SMART functional defects at a distance of 40 mm gets touched by mainly twin grains. The monocrystalline ingot volume as observed in the investigated ingot samples has been completely free of parasitic grains. The results imply that the modification of the crystallographic characteristic of the grain boundary by the twinned grains is not that significant that it enables the leapfrogging of grains over the SMART induced grain boundaries into the monocrystalline region.

Within the region left of the functional defects, the grain boundaries of the multicrystalline region are visible as line structures of slightly reduced lifetime in the PL image. The grain boundaries induced by the SMART seeding grow as almost parallel vertical lines. In the upper image part, a dislocation tangle is visible within the two grain boundaries. This is the desired effect of the small angle grain boundary within the functional defect region to induce dislocations. On the right hand side of the functional defects, no extended crystal defect structures can be observed. Only a few recombination active structures in the vicinity of the grain boundary indicate that the intended dislocation confinement within the two large angle grain boundaries did not fully hold.

From the adjacent brick in the monocrystalline regions, selected wafers were processed as described in paragraph 2.3 and analyzed by QSSPC measurements. For wafers from the middle and upper height of this p-type ingot, values between 1.5 ms and 0.9 ms at $\Delta n = 1 \times 10^{15}$ cm^{-3} for a base resistivity ρ between 1.5 Ωcm and 1.2 Ωcm were measured. QSSPC measurements of a Cz-Si reference wafer with a resistivity of 1.3 Ωcm after the same processing steps revealed lifetime values of about 1.3 ms. By that comparison it is shown that this p-type block cast material features comparable lifetime values to Cz-Si material and proves that this type of material is well suited for processing of high efficient PERC solar cells.

3.3 Industrial perspective for seeding variants

The use of the SMART seeding technique shows the potential to significantly enhance the material quality in the G2 sized ingots. When using seeding configuration "mod. SMART", a very efficient blocking of the parasitic grains is reached. For transfer into industrial processes the size of the small mono plate would have to be adapted to the ability of the furnace to provide a thermal field inducing a convex growth interphase near the crucible wall while maintaining low thermal stresses. The outer border of the bricks would then be at the position of the SMART grain boundaries. Thus the overall ingot and crucible size would have to be adapted to this enlargement of lateral dimensions. Since the standard edge size of silicon wafers for solar cells is actually under revision and a change of the crucible size mandatory anyway, these changes might be beneficial without adding cost to the overall process.

By the use of a SMART seeding stack between all large seed plates, it is possible to use just one type of monocrystalline plates with a <100> orientation in growth direction and the same orientation of the side faces. This is cost effective for the preparation of the large monocrystalline seed plates, because only one type of silicon plate is needed. Since the functional defect region grows vertical from bottom to top with only a small lateral enlargement, the cutting scheme for the production of bricks can be adapted such that most of the defect region is cut away during the bricking and grinding process. Thus high quality wafer can be produced based on the directional solidification process. However, the complexity for the preparation of the small SMART plates and the seeding procedure itself may increase the overall cost significantly. Therefore, in order to successfully transfer the concept into an industrial process, the reusability of the seed layer is of major importance and has to be studied in further work.

4 CONCLUSION

Different seeding techniques for block casting of cast-mono material were evaluated regarding the material quality. The introduction of functional defects according to the SMART approach enabled a significant reduction of structural defects. The ingrowth of parasitic grains could be stopped for the lower third of the ingot and dislocation clusters spread less than in standard cast-mono material. This improved the mean lifetime on n-type passivated wafers to ~1.2 ms at a resistivity of 0.9 Ωcm in contrast to ~0.8 ms for the cast-mono material. The new approach introducing a monocrystalline spacer is very promising as the avoidance of the ingrowth of parasitic grains was successful over the whole ingot height. In p-type material, lifetimes up to 1.5 ms for resistivities of 1.2 - 1.5 Ωcm after high temperature processing have been observed. Therefore the SMART seeding technology

shows a high potential for the successful industrialization of cast-mono processes.

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6 REFERENCES

[1] A. W. Blakers, A. Wang, A. M. Milne, J. Zhao, and M. A. Green, "22.8% efficient silicon solar cell," *Appl. Phys. Lett.*, vol. 55, no. 13, pp. 1363–1365, 1989.

[2] N. S. Pujari *et al.*, "International Technology Roadmap for Photovoltaic(ITRPV)," 2018. [Online] Available: http://www.itrpv.net/. Accessed on: Jul. 23 2018.

[3] C. W. Lan *et al.*, "The emergence of high-performance multi-crystalline silicon in photovoltaics," *J. Cryst. Growth*, vol. 468, pp. 17–23, 2017.

[4] F. Schindler *et al.*, "Towards the efficiency limits of multicrystalline silicon solar cells," *Sol. Energy Mater. Sol. Cells*, vol. 185, pp. 198–204, 2018.

[5] N. G. Stoddard *et al.*, "Casting Single Crystal Silicon: Novel Defect Profiles from BP Solar's Mono^2 TM Wafers," *Solid State Phen.*, vol. 131-133, pp. 1–8, 2008.

[6] K. Kutsukake, N. Usami, Y. Ohno, Y. Tokumoto, and I. Yonenaga, "Control of Grain Boundary Propagation in Mono-Like Si: Utilization of Functional Grain Boundaries," *Appl. Phys. Express*, vol. 6, p. 25505, 2013.

[7] I. Takahashi, S. Joonwichien, T. Iwata, and N. Usami, "Seed manipulation for artificially controlled defect technique in new growth method for quasi-monocrystalline Si ingot based on casting," *Appl. Phys. Express*, vol. 8, no. 10, p. 105501, 2015.

[8] J. A. Giesecke, M. C. Schubert, F. Schindler, and W. Warta, "Harmonically Modulated Luminescence: Bridging Gaps in Carrier Lifetime Metrology Across the PV Processing Chain," *IEEE J. Photovoltaics*, vol. 5, no. 1, pp. 313–319, 2015.

[9] J. A. Giesecke, R. A. Sinton, M. C. Schubert, S. Riepe, and W. Warta, "Determination of Bulk Lifetime and Surface Recombination Velocity of Silicon Ingots From Dynamic Photoluminescence," *IEEE J. Photovoltaics*, vol. 3, no. 4, pp. 1311–1318, 2013.

[10] J. Giesecke, M. C. Schubert, B. Michl, F. Schindler, and W. Warta, "Minority carrier lifetime imaging of silicon wafers calibrated by quasi-steady-state photoluminescence," *Sol. Energy Mater. Sol. Cells*, vol. 95, no. 3, pp. 1011–1018, 2011.

[11] R. A. Sinton and A. Cuevas, "Contactless determination of current–voltage characteristics and minority-carrier lifetimes in semiconductors from quasi-steady-state photoconductance data," *Appl. Phys. Lett.*, vol. 69, no. 17, pp. 2510–2512, 1996.

[12] B. Gao *et al.*, "Reduction of polycrystalline grains region near the crucible wall during seeded growth of monocrystalline silicon in a unidirectional solidification furnace," *J. Cryst. Growth*, vol. 352, no. 1, pp. 47–52, 2012.

[13] Y. Miyamura *et al.*, "Crystal growth of 50 cm square mono-like Si by directional solidification and its characterization," *J. Cryst. Growth*, vol. 401, pp. 133–136, 2014.

[14] X. Zhang, L. Gong, B. Wu, M. Zhou, and B. Dai, "Characteristics and value enhancement of cast silicon ingots," *Sol. Energy Mater. Sol. Cells*, vol. 139, pp. 27–33, 2015.

[15] V. A. de Oliveira *et al.*, "Sub-grain boundaries sources and effects in large mono-like silicon ingots for PV," 2014.

[16] D. Hu *et al.*, "The characteristics of sub-grains in the mono-like silicon crystals grown with directional solidification method," in *38th IEEE Photovoltaic Specialists Conference*, Austin, Texas, 2012, pp. 2735–2738.