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INFLUENCE OF THE TRANSPARENT ELECTRODE SPUTTERING PROCESS ON THE INTERFACE PASSIVATION QUALITY OF SILICON HETEROJUNCTION SOLAR CELLS

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ABSTRACT: The efficiency of silicon heterojunction solar cells is limited by the parasitic absorption within the intrinsic and doped hydrogenated amorphous silicon (a-Si:H) layers, hence minimizing their thickness by simultaneously preserving the high-level passivation quality is crucial. The a-Si:H must withstand subsequent processing steps, in particular the deposition of a transparent electrode. Here sputter deposition of transparent conducting oxides (TCOs) is commonly the method of choice, since this well established technique can yield uniform TCO layers with suitable electrical and optical properties. This paper aims at the design of a soft sputter deposition process, which allows utilizing well established DC magnetron sputtering on top of ultrathin a-Si:H layers, without a significant degradation of passivation quality. For this purpose, the influence of the a-Si:H thickness, the chamber pressure and the applied power are reviewed for In_2O_3:Sn (ITO) deposition. As a simple approach to combine excellent surface passivation, acceptable electrical TCO bulk properties and high throughput, an ITO double layer stack, featuring a few nanometers thin softly deposited intermediate ITO layer below a high rate deposited thicker ITO layer, is presented. Hereby the implied open-circuit voltage of test structures could be improved by almost 30 mV.

Keywords: TCO transparent conducting oxides, sputtering, heterojunction

1 INTRODUCTION

Silicon heterojunction (SHJ) solar cells receive more and more attention in recent years due to their high performance potential, owing to the effective absorber surface passivation capability of hydrogenated amorphous silicon (a-Si:H). The SHJ design, consisting of a monocrystalline silicon (c-Si) wafer (most commonly n-type) sandwiched between few nanometers thick intrinsic a-Si:H followed by a doped a-Si:H layer on each side, forming the emitter (p-type) and the back-surface field (n-type), enables record open-circuit voltages V_{oc} without the need for complex patterning steps [1]. Unfortunately, the intrinsic (*i*) and doped (*p*,*n*) a-Si:H layers absorb light parasitically, meaning that the charge carriers generated here contribute only marginally to the short-circuit current (J_{sc}) [2]. In [3] optimum *i* and *p*-layer thicknesses of 4 and 3 nm are reported, respectively, because no gain in the resulting V_{oc} and fill factor *FF* is achievable for thicker layers and the J_{sc} decreases gradually.

As the conductivity within the amorphous layers is low, transparent electrodes are deposited on top to facilitate lateral charge transport to the local metal contacts. For this purpose tin doped indium oxide In_2O_3:Sn (ITO) is a widespread transparent conducting oxide (TCO) and the highest quality films have routinely been produced via the magnetron sputtering technique [4]. Magnetron sputtering is also an appealing approach for the deposition of a high work function oxide of transition metals like Molybdenum or Tungsten [5]. A highly transparent film thereof can be used as a replacement for the p-type a-Si:H emitter layer and will be deposited directly on the a-Si:H(i) passivation layer. In general, during such sputtering processes the substrates are exposed to high-energy particles (sputtered atoms, reflected neutrals, ions and electrons with kinetic energies of up to the target voltage multiplied by the elementary charge) as well as to plasma radiation, which modify the nanometer thin layers and interfaces below and can lead to a strong increase in recombination and thus to a loss in V_{oc} and potentially in *FF*.

Monte Carlo simulations via the Stopping and Range of Ions in Matter (SRIM) software [6] (Fig. 1) estimated that oxygen ions O^-, which are expected to be the majority species of negatively charged ions incident on the substrate [7], can penetrate up to 7 nm deep into the a-Si:H film when accelerated by voltages of the order of the target – substrate voltage (e.g. 252 V for the 40 W process considered later). The penetration depth of argon atoms of the same energy, coming from the target after reflection and neutralization, is slightly smaller, due to their larger atomic diameter. It can be assumed that the sputtering processes can lead to significant damages to a depth of roughly 10 nm within the passivation layer and the a-Si:H / c-Si interface region.

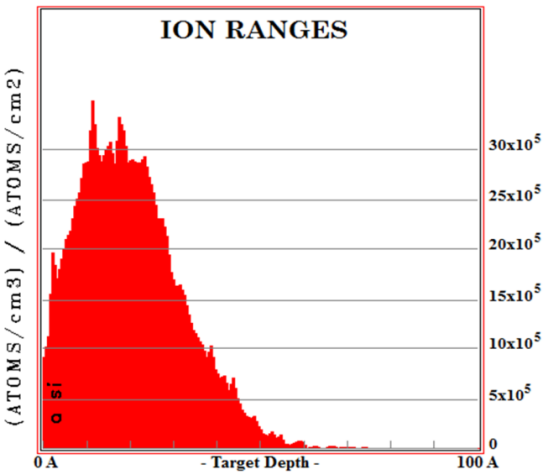

Figure 1: SRIM Monte Carlo simulation for the penetration depth of oxygen atoms with an initial kinetic energy of 252 eV in a-Si:H. The amount of oxygen atoms within a cubic centimeter of a-Si:H, normed by the number of impacting particles per area, is shown for a depth of up to 100 angstrom below the surface.

According to the simulations those damages do not only consist of broken atomic bonds, but also of atomic defects, which are hardly or not at all remediable by the low temperature annealing procedure typically applied for SHJ cells.
Varying the applied power and the chamber pressure enables to control the flux and energy of the involved particles, which significantly influences the growth and thus the properties of the resulting films, as well as the hereby caused passivation degradation. This paper aims at investigating the influence of these two externally controllable parameters on the sputter-induced a-Si:H / c-Si recombination losses.
Depositing the first nanometers of ITO in a relatively gentle and slow sputter process, followed by a thicker layer at a high growth rate, turned out to be a reasonable compromise between passivation degradation, electrical TCO bulk properties (sheet resistance, charge carrier mobility and density) and process duration.

2 EXPERIMENTAL

Planar n-type float-zone c-Si wafers with a thickness of 200 µm and a resistivity of 1 Ωcm were used to quantify the degradation of the passivation quality during ITO sputter deposition. The wafers were cleaned according to the RCA cleaning procedure. After the final HF dip, the a-Si:H(i) was deposited by means of plasma-enhanced chemical vapor deposition (PECVD). After activating the c-Si / a-Si:H(i) interface passivation in a 200 °C step for 10 minutes on a hotplate at ambient air, all samples had minority charge carrier (mc) lifetimes of a few milliseconds at an injection level of 10^{15} cm^{-3}. For faster processing, some of the rear sides of the samples were coated by well-passivating silicon nitride (SiN_x). Lifetimes were always determined via photo conductance measured by the Sinton WCT-120 tool operated in generalized mode [8].
For higher sensitivity and simplification of the process sequence, doped a-Si:H layers, which are usually applied to form junctions vital for charge carrier separation in solar cells, are omitted in these lifetime samples. Thus the about 75 nm thick ITO is expected to induce a band bending within the absorber and the resulting field effect is likely to influence the charge carrier recombination at the interface to some extent. Nevertheless, since trends in the chemical passivation capability as a function of the preceding sputter processes are observable and in order to be closer to the actual cell, ITO was not etched after its deposition.
The DC magnetron sputtering was performed by an Oxford Instruments cluster tool using a circular ITO target with a composition of In_2O_3/SnO_2: 90/10 weight percent, a diameter of 25.4 cm and a purity of 99.99 %. The gap between target and the sample is about 10 cm. Besides the argon and oxygen flows, the total pressure within the process chamber can be set by means of restricting the pump capacity by a butterfly valve. Hereby a relatively large pressure of up to 85 mTorr can be reached. The substrate holder is continuously heated to 100°C.
Providing good access to quantify the sputter-induced degradation of the interface passivation, the mc lifetime within the passivated c-Si wafer at a fixed minority charge carrier density (mcd = 10^{15} cm^{-3}, if not stated otherwise), was consistently measured before ITO deposition, afterwards and subsequent to an annealing step on a hotplate. The mc lifetime generally shows similar trends as the implied V_{oc} (iV_{oc}) at 1 sun illumination, which is a key performance indicator of a potential solar cell. Every data point represents the average of two samples taken from different wafers and the error bars indicate the standard deviation.

3 RESULTS AND DISCUSSION

3.1 Impact of the a-Si:H(i) layer thickness

In order to evaluate the passivation capability, the standard baseline ITO DC magnetron sputtering process (referred to as ITO std) was applied to double-side passivated planar c-Si wafers, whereby the a-Si:H(i) thickness on the side to be ITO coated was varied. The ITO std recipe, whose main parameters are a sputtering power of 200 W, 2 mTorr chamber pressure, a growth rate of 0.44 nm/s and argon and oxygen flows of 30 and 0.7 sccm respectively, is selected due to moderate damage for above 10 nm thick a-Si:H layer stacks and good electrical bulk properties of the resulting ITO film. Those are a charge carrier mobility μ of above 40 cm^2/Vs at a charge carrier density of around 10^{20} cm^{-3}, leading to a sheet resistance of less than 300 Ω/□ for a 75 nm thick film.
Fig. 2 shows that the initial mc lifetimes and the degree of sputter-induced degradation are highly dependent on the a-Si:H(i) layer thickness. The level of surface passivation before sputtering saturates for about 7 nm thick films on a solid level of around 3 ms. While the sputter-induced deterioration of the passivation gradually decreases with a-Si:H(i) layer thickness, low temperature annealing allows to partly cure this damage for films > 7 nm and a similar level is obtained for 12, 18 and 23 nm.

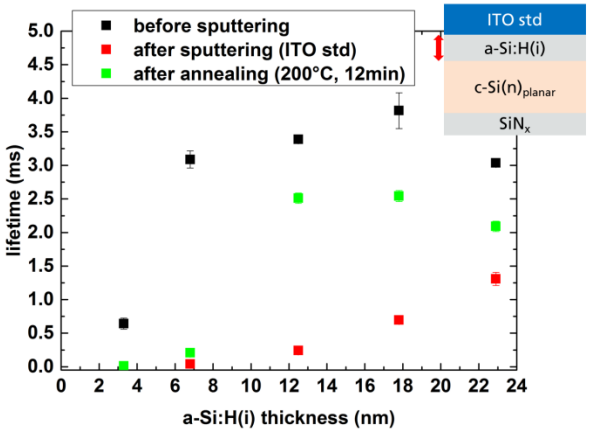

Figure 2: Minority charge carrier lifetimes for various a-Si:H(i) layer thicknesses before (black squares) and after (red squares) ITO deposition and a subsequent annealing (green squares).

In a-Si:H the penetration depth of energetic particles (here primary sputtered atoms, reflected neutrals and ions at energies of up to the target voltage multiplied by the elementary charge) can be estimated to be smaller than 10 nm (Fig. 1). Hence for the thicker a-Si:H(i) layers, only a negligible amount of harmful particles is expected to arrive at the vicinity of the a-Si / c-Si interface. Furthermore, the absorption length of ultra violet

radiation of 350 nm wavelength amounts about 10 nm in amorphous silicon [9]. This photon energy corresponds to the strength of the passivating Si-H bonds at the c-Si surface and is thus able to degrade the passivation quality.
However, to conclude, the ITO std sputtering process is unsuited to preserve the excellent surface passivation of 7 nm a-Si:H(i) films, which calls for an adjustment of the procedure.

3.2 Influence of the applied sputtering power

To isolate the impact of the applied power, ITO was deposited on 8 nm thick a-Si:H(i) layers under otherwise equal process conditions. The power was varied from 200 W (std) to 40 W and 500 W (Fig. 3), coming along with a change in the corresponding growth rates and cathode voltages, depicted in Tab. 1. Decreasing the power to 40 W softens the process clearly, visible in the lifetimes measured after sputtering and more pronounced in the values taken after the annealing steps. Annealing the samples at 210 °C showed a slight enhancement of the mc lifetime compared to the preceding 180 °C step whereas annealing at further elevated temperatures (not shown) was detrimental.
The difference in ITO deposition-induced damage between the 200 W and the 500 W processes is present, but far less significant.

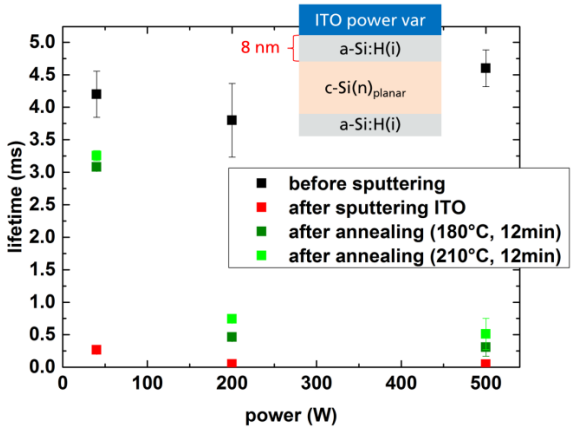

Figure 3: Lifetimes before and after sputtering at different power and after consecutive annealing steps at 180 and 210 °C.

During low power processes, a lower amount of harmful particles hit the substrate per time unit, indicated by the lower deposition rate (Tab. 1) and the sputter current (power divided by cathode voltage) and also the plasma radiation is less dense.

Table I: Deposition rate and DC target voltage for various power and pressure settings

Power [W]	**Pressure** [mTorr]	**Rate** [nm/s]	**DC Voltage** [V]
40	2	0.072	252
200	2	0.44	283
500	2	1.16	313
200	5	0.38	295
200	10	0.277	305
200	20	0.18	315
200	40	0.068	324
200	85	0.018	330

While this is likely compensated by the extended deposition duration to get the same thickness of about 75 nm, the applied power also determines the maximum kinetic energy of the sputtered atoms and reflected neutrals, since it correlates with the target voltage. This limitation of the impact energy and the consequential penetration depth could be a reason for the less severe passivation damage, but probably not the complete explanation, since the reduction in target voltage between the 200 W and the 40 W process amounts only 11 %. Here a further and more detailed investigation is necessary, e.g. by means of plasma analysis.
However, in terms of throughput, reducing the growth rate for the ITO single layer is not a suitable solution.

3.3 Influence of the total chamber pressure

In a next step the total chamber pressure was varied at a constant power of 200 W (Fig. 4). To improve comparability, the measured minority carrier lifetimes are normalized by the related pre-sputtering values, which were on the same level for all samples. A clear tendency of lower degradation for higher process pressures is observable, which is more pronounced after annealing. Although the DC voltage increases with pressure (Tab. 1), particles arrive at the substrate surface with quite low velocities, due to collisions within the denser gas. At the high pressure of 85 mTorr and for the geometry of our sputter system, the plasma between target and substrate is dense enough to thermalize almost all energetic particles coming from the cathode [10]. For these high pressure processes the remaining damage, likely primary induced by plasma radiation, could be cured virtually completely in a 200 °C step.
Unfortunately, films grown under these conditions show relatively poor electronic bulk properties as discussed in the next subsection. Since also process durations are increased by a multiple, depositing the whole ITO layer at a high pressure will neither lead to a better solar cell performance nor be an economically attractive process.

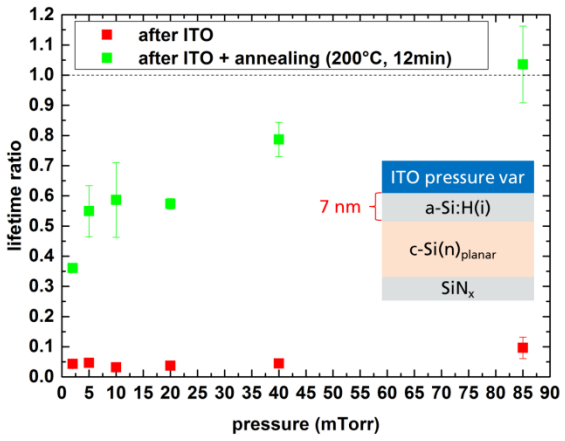

Figure 4: Minority carrier lifetimes after ITO sputter processes at various chamber pressures and subsequent to annealing. The values are normalized by the individual initial pre-sputter mc lifetime (at a level of 1.5 ms) to simplify comparison.

3.4 Inserting a softly deposited intermediate ITO layer

Taking advantage of the softer sputter process at either low power or high pressure, these layers were combined with the standard ITO procedure in a 75 nm thick layer stack, with the aim of enhancing electrical

bulk properties of the film and to shorten deposition durations. Fig. 5 shows a comparison with regard to sputter-induced degradation of five recipes, namely (i) a single layer of the standard ITO (sl_std), (ii) a single layer with a reduced power of 40 W (sl_low_power), (iii) a single layer at an enhanced pressure of 85 mTorr (sl_high_pressure) and two layer stacks consisting of a 20 nm layer deposited at (iv) either 40 W (stack_power) or (v) 85 mTorr (stack_pressure) followed by 55 nm ITO std, summarized in Tab. 2.

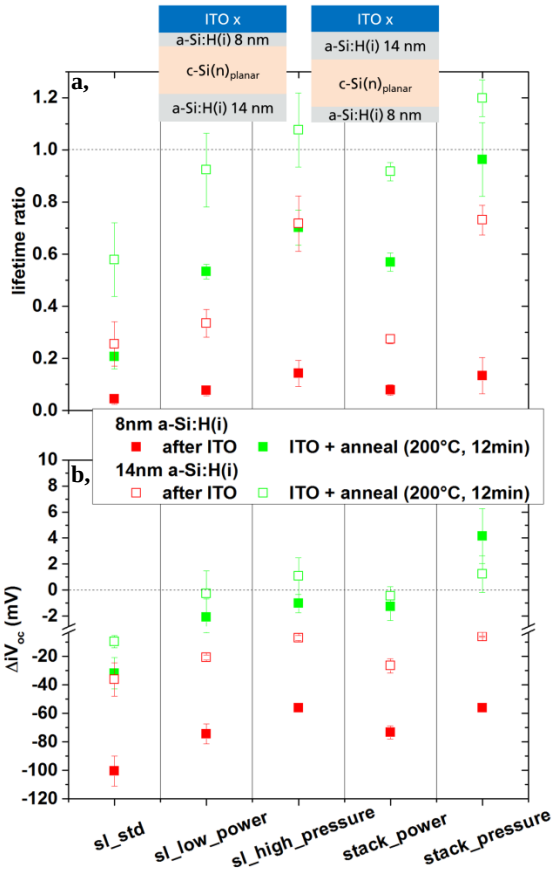

Figure 5: Normalized mc lifetimes (a) and change in iV_{oc} (b) during sputtering and annealing for five ITO deposition recipes (listed in Tab. 2) applied on a-Si:H(i) passivation layers of 8 nm (filled squares) and 14 nm (empty squares) thickness.

Table 2: ITO sputter recipes evaluated in Figs. 5 and 6

Name	Power [W]	Pressure [mTorr]	Duration [min:sec]
sl_std	200	2	03:10
sl_low_power	40	2	16:12
sl_high_pressure	200	85	64:49
stack_power	40	2	04:38
	+ 200	2	02:16
stack_pressure	200	85	18:31
	+ 200	2	02:16

The processes were applied for a single-sided ITO coating of lifetime samples with asymmetrically thick (8 and 14 nm) a-Si:H(i) layers on both sides. Before sputtering, this resulted in initial mc lifetimes of around 2 ms and an iV_{oc} level of 726 ± 3 mV. By this means the sputter impact can be evaluated for two passivation layer thicknesses by depositing on top of one of the two opposing sample sides. The difference in iV_{oc} before and after sputtering ΔiV_{oc} (Fig. 5b) shows the same trends as the post-sputter mc lifetime normalized by the initial values (Fig. 5a). Even after annealing, the reference ITO procedure (sl_std) causes a loss of 30 mV for a coating of the 8 nm thick a-Si:H(i) layer. For the single ITO layers deposited under soft process conditions as well as for the ITO double layer stacks, the degradation is less than 2 mV after annealing.

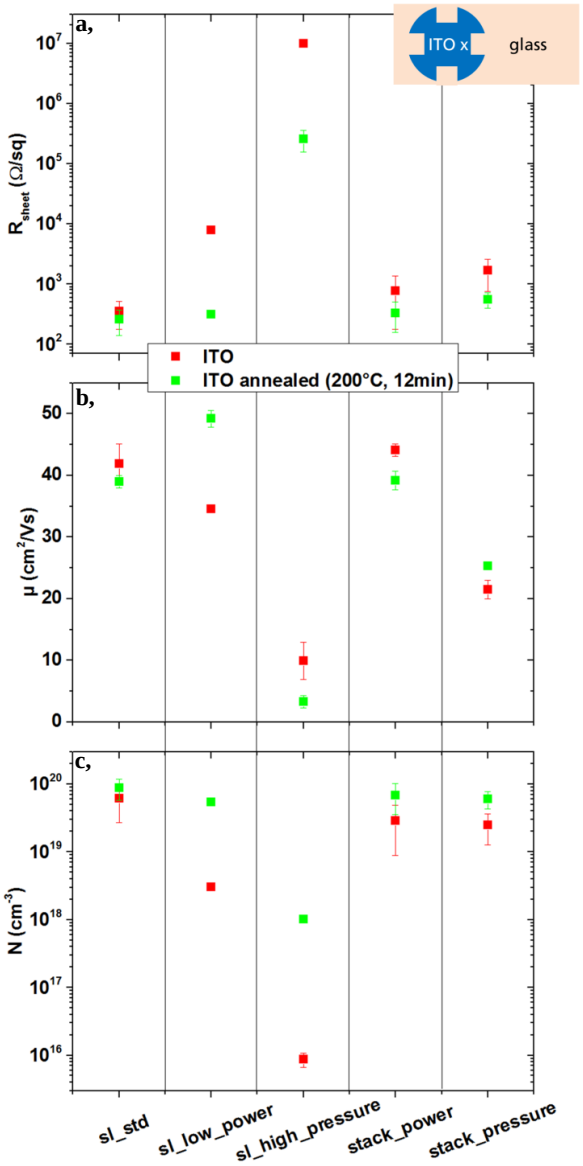

Figure 6: Electrical film properties sheet resistance (a), charge carrier mobility (b) and concentration (c) of 75 nm thick ITO deposited on glass according to the recipes in Tab. 2 and subsequent to an annealing step at 200 °C, measured via the van der Pauw method.

A similar effect is observable for the 14 nm thick a-Si:H(i) layer, whereby this layer is less sensitive to sputter damage, visible in the smaller absolute value of ΔiV_{oc} for every process.
The main message from this comparison is that it suffices to sputter a nanometer thin protective layer gently before the residual ITO follows by harsh process conditions optimized for bulk properties and a high growth rate.

In Fig. 6 the corresponding electrical bulk properties of the ITO films deposited on glass are shown. The sheet resistance and the mobility and density of the charge carriers are determined via the van der Pauw method using the Hall Effect. Although the films grown on glass substrates do not utterly resemble the ones within the SHJ cell, it can be concluded that the high pressure deposited ITO cannot match the good electrical properties provided by the standard process. The values for sheet resistance and charge carrier mobility of the annealed high / low pressure layer stack (stack_pressure) (R_{sheet} = 550 Ω/□, μ = 25 cm²/Vs) are in between the high pressure single layer (sl_high_pressure) (R_{sheet} = 2.5x10^5 Ω/□, μ = 3 cm²/Vs) and the standard ITO film (sl_std), but slightly worse than one might expect by treating the layer stack as a parallel circuit of the two ITO films. This suggests that the adverse growth of the 20 nm thick low-rate deposited protective layer continues for a while in the subsequent standard processed film.

For the film sputtered at low power and also for the related layer stack, the electrical properties are at a similar level as for the ITO std process. Remarkably, the charge carrier mobility within the annealed film deposited at 40 W reaches the value of 50 cm²/Vs.

However, the prolonged process durations of the gently deposited films and the poor electrical properties of the high pressure layers motivate to reduce their thickness to a minimum necessary to function as an effective protection layer. For this purpose the sputter-induced degradation is quantified in Fig. 7 as a function of the thickness of this intermediate layer deposited at 85 mTorr for 7 nm thick a-Si:H(i) films with initial mc lifetimes of around 1.5 ms.

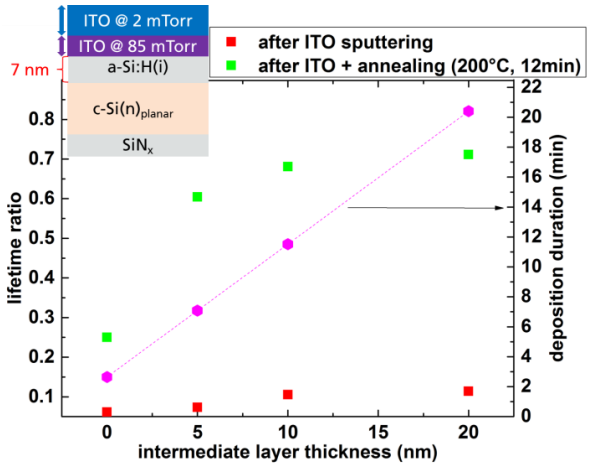

Figure 7: Influence of the thickness of the gently deposited protective ITO layer on the sputter-induced degradation and the process duration of the entire ITO film. The soft layer was deposited at 85 mTorr and 200 W, before the remaining ITO to build a 75 nm thick film followed under standard conditions (2 mTorr, 200 W).

Already a 5 nm thick ITO shielding is sufficient to increase the normalized mc lifetimes after sputtering and annealing at 200 °C by a factor of 2.4, compared to the deposition without intermediate layer. Thicker protective layers (10 nm and 20 nm) prevent sputter-induced degradation slightly further. In contrast to the previous experiment (Fig. 5), this time annealing could not boost the mc lifetime to the full initial value for the 20 nm protective ITO layer, which can be due to a slight variation in the process chain or in the annealing procedure. Nevertheless, when a gently deposited layer is present, the sputter-induced loss in iV_{oc} was merely between 2 and 4 mV (at an initial level of 715 ± 2 mV). Hence, surface passivation can be much better preserved during the sputter deposition, which here resulted in an iV_{oc} improvement of 26 mV in comparison to the standard ITO single layer.

4 CONCLUSION

As was estimated by SRIM simulations, the highest-energy atoms present during ITO sputter coating are able to modify the underlying a-Si:H film and the interface region to the c-Si absorber up to a depth of 10 nm below the substrate surface. Since the optimum thickness of the intrinsic / doped charge carrier selective a-Si:H layer stack is of the same order, the excellent interface passivation quality is highly sensitive to the sputtering process conditions, in particular the applied power and the chamber pressure. Both a decrease in power down to 40 W and an enhanced pressure of 85 mTorr, compared to the (200 W, 2 mTorr) standard process, showed a significant decrease in sputter-induced damage and the resulting degradation in iV_{oc} was almost completely remediable during low temperature curing. While the low power process also yielded an ITO film with good electrical properties, the high pressure turned out to be detrimental for the layer growth, resulting in a high resistivity. It has to be mentioned that these processes were not optimized yet and reducing the oxygen flow during the high pressure ITO deposition will likely enhance the charge carrier concentration within the TCO layer and thereby lower its sheet resistance.

Applying these gently deposited layers as a shielding in a stack previous to the standard ITO process is an effective way to alleviate sputter-induced degradation by a multiple. At least for the low / high power ITO stack, a good compromise between preserving the absorber passivation, good electrical bulk properties of the TCO film and a reasonable process duration was achieved.

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