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LASER-TRANSFERRED NI-SEED FOR THE METALLIZATION OF SILICON HETEROJUNCTION SOLAR CELLS BY CU-PLATING

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ABSTRACT: We present results about a laser-based method for the metallization of silicon heterojunction solar cells by Cu-plating. The method consists of first depositing a dielectric layer as plating mask onto the transparent conductive oxide (TCO) and then depositing a NiV seed layer onto the plating mask by laser induced forward transfer (LIFT). Afterwards, the seed layer is fired through the plating mask in a second laser step in order to form a contact to the TCO. By dividing the process into laser transfer and firing (LTF) each step can be optimized separately. The final metallization is produced by Cu-plating. A pulse plating process is applied to further reduce parasitic plating. Different dielectric layers are tested as plating masks for their resistance against parasitic plating. The combination of a 15 nm thick Al_2O_3 layer as plating mask in conjunction with pulse plating is completely free of parasitic plating. Finally an efficiency of 22.2% is reached outperforming the screen printed reference cells by $0.5\%_{abs}$.

Keywords: Laser Processing, Heterojunction, Metallization, Plating

1. INTRODUCTION

Cu-plating as a low-temperature process is well suited for the metallization of silicon heterojunction (SHJ) solar cells, due to their temperature-sensitive passivation. Kaneka has demonstrated an efficiency of 25.1% with a plated SHJ solar cell [1], which represents the efficiency record for both-side contacted SHJ solar cells and is higher than any reported result of solar cells with screen printed contacts.

Screen printing is the most used method for the metallization of silicon homojunction solar cells. After decades of continuous development it has proved to be a robust method with a high performance. But due to the firing temperatures > 700°C it is not directly applicable to SHJ solar cells. Special low-temperature pastes have to be used, which feature a much higher resistivity of the cured fingers [2]. The resistivity of Cu-plating, on the other hand, is close to that of bulk Cu. Furthermore, with plating it is possible to produce thinner fingers compared to screen printed fingers.

With respect to adhesion, low-temperature pastes did not yet undergo the same development as the high-temperature pastes and in fact in many cases the requested peel force of 1 N/mm with soldered ribbons is not reached [3]. Also the development of Cu-plating on transparent conductive oxides (TCO) is still at the beginning, but with an appropriate intermediate layer between the TCO and the plated Cu high peel forces between 3 and 5 N/mm have already been measured [4, 5].

Plating a metal grid on the TCO of SHJ solar cells requires a negative plating mask that defines the shape of the grid, because otherwise the whole TCO area would be plated. Many approaches use patterned organic masks for this purpose [4, 6, 7, 7–11]. These masks, however, have to be removed after the plating process. But the coating materials and the waste water management for chemically removing the mask are quite expensive.

An approach based on a SiO_x plating mask was presented by Adachi et al. [12] and patented by Kaneka [13]. The advantage of this sequence is that the SiO_x layer remains on the cell. The SiO_x layer, however, cannot be deposited in the same tool as the TCO, because one part of the metallization is applied before the SiO_x layer. And since screen printing and plating are combined the lowest achievable finger width is defined by the screen printing finger width.

The use of laser processes for structuring a dielectric plating mask, as it is done for homojunction solar cells [14], would be a preferable choice. But since the dielectric layer and the TCO are both transparent for laser wavelengths in the suitable spectrum, such processes are

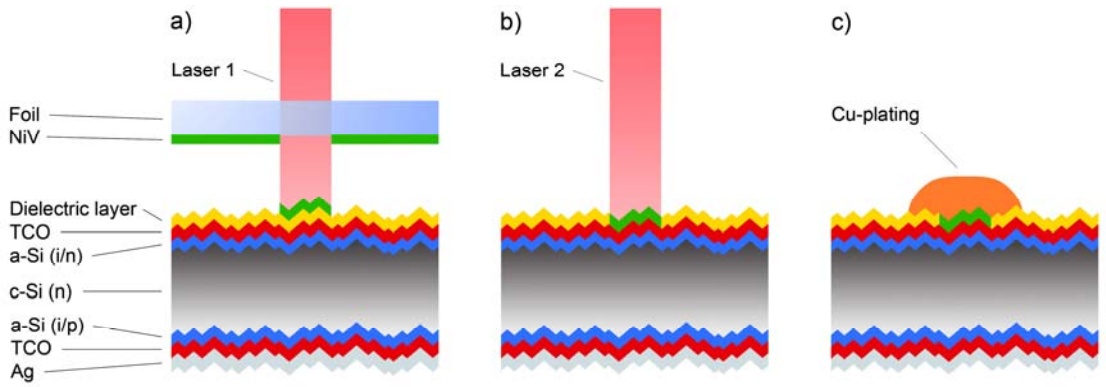

Figure 1: Schematic view of the laser transfer and firing (LTF) process sequence followed by plating, a) laser induced forward transfer (LIFT), b) laser firing, c) plating [15]

not easily applicable for SHJ solar cells. A recently presented laser structuring approach uses an amorphous silicon (a-Si) layer on the dielectric plating mask, which acts as absorption layer for the laser irradiation [16]. The absorption layer, however, has to be removed after plating, which makes the process rather expensive.

In this paper, we present results about a method for plating on SHJ solar cells with a laser structured dielectric plating mask, in which the plating mask can in principle be deposited in the same tool as the TCO and all deposited layers can remain on the finished solar cell. The method is based on laser induced forward transfer (LIFT) [17] and is described in detail in [15].

Different dielectric layers were tested for their resistance against parasitic plating. Furthermore we produced (156x156) mm² solar cells with the LTF and plating approach and compared them to screen printed solar cells.

2. APPROACH

A scheme of the process sequence can be seen in figure 1. A dielectric layer is deposited on the TCO as plating mask. A NiV seed layer grid is deposited by LIFT onto the dielectric layer using inexpensive plastic foil as LIFT carrier substrate. After LIFT the foil is removed and in a second laser step the seed layer is fired to form a contact to the TCO. The metallization is then formed by plating on the seed layer grid, while the dielectric plating mask also protects the TCO from the acidic electrolyte.

The separation of the laser process into laser transfer and firing (LTF) allows for a separate optimization of the two steps. As it was shown in [15] the two steps do not need to be precisely aligned to each other.

We used a reverse pulse plating process to enhance the plating selectivity and thereby reduce parasitic plating [18]. Instead of direct current (DC) we alternatingly applied forward and reverse pulses. During the forward pulses the plated metal grows faster on the seed layer than on the plating mask, because on the plating mask the ions need more time to diffuse to the rare defect sites, where they are eventually deposited. During the reverse pulses, on the other hand, the small nuclei that have formed during the previous forward pulse on the plating mask are completely dissolved, while on the seed layer the metal that has been deposited during the previous forward pulse is only partially dissolved.

3. EXPERIMENTAL

The carrier foils for the LIFT process were 100 µm thick biaxially-oriented polyethylene terephthalate (BoPET) foils. 100 nm NiV (with 7 wt% vanadium) were sputtered on one side of the foils. For laser transfer and laser firing we used a laser with 1064nm wavelength and 15 ns pulse length. The Gaussian laser beam had a diameter of 20 µm in the focal plane. The laser beams for transfer and firing were accurately aligned to each other.

We used non-metallized industrial (156x156) mm² Cz n-type SHJ precursors with indium tin oxide (ITO) as TCO. The front side structure was a-Si(i)/a-Si(n)/ITO and the back side structure a-Si(i)/a-Si(p)/ITO. Both wafer sides were textured.

We deposited different dielectric layers on the front side ITO as plating masks. The tested materials were Al_2O_3 deposited by atomic layer deposition (ALD) and SiN_x deposited by sputtering and plasma enhanced chemical vapor deposition (PECVD). The effect of the deposition on the passivation was measured by a comparison of photoluminscence (PL) images before and after the deposition from which the change of the implied open circuit voltage (V_{OC}) was calculated [15]. The back side metallization was produced by evaporating 1 µm of Ag. The front was metallized by the LTF sequence followed by Cu-plating in a RENA inline-tool, in which only the front side is wetted by the copper sulfate based plating bath and the cell is illuminated from the front side and contacted on the rear side. After the Cu plating a thin Ag capping was plated onto the copper. We also produced reference solar cells with a screen printed low-temperature paste metallization [19], which was printed on the front side ITO of the precursors and cured for 9 min at 200°C. The back side of the reference cells was also fully metallized with 1 µm evaporated Ag.

4. RESULTS AND DISCUSSION

Different dielectric layers were deposited on the ITO of the precursors as plating masks to test their resistance against parasitic plating and to measure the V_{OC} change caused by the deposition. The parasitic plating after Cu-plating was qualitatively categorized (low, mid, high). Even though with standard DC-plating more parasitic plating was expected, we used it for this test instead of pulse plating, because the aim was just to compare the different dielectric layers.

Table I: Dielectric layers tested for their resistance against parasitic plating with DC plating

Layer	Deposition temperature (°C)	Thickness (nm)	Parasitic plating	ΔVoc (mV)
Al_2O_3 (ALD)	180	20	low	0
Al_2O_3 (ALD)	180	15	low	0
Al_2O_3 (ALD)	180	11	low	0
Al_2O_3 (ALD)	180	7	mid	0
Al_2O_3 (ALD)	180	3	mid	0
SiN_x (PECVD)	300	15	mid	-10
SiN_x (sputtered)	150	15	high	1

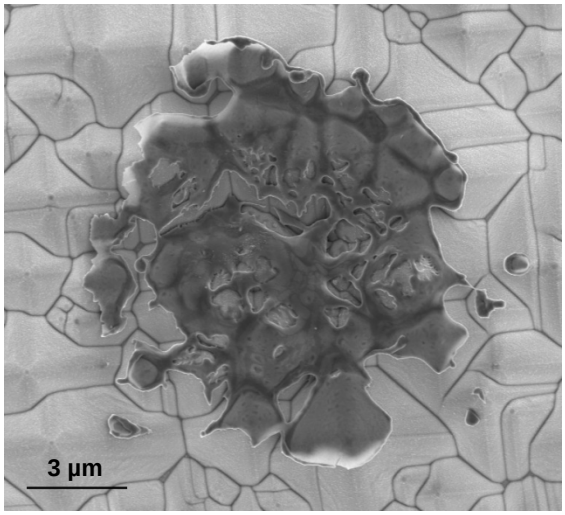

Figure 2: SEM image of NiV LIFT spot on a SHJ precursor coated with 15nm Al_2O_3 produced with a LIFT fluence of 0.25 J/cm^2.

The results are listed in table 1. For all layers except the PECVD layer only a negligible implied V_{OC} change was measured. This can be explained with the deposition temperatures which are also listed in the table. The highest temperature was used for PECVD.

For Al_2O_3 layers with a thickness of 11 nm or higher only weak parasitic plating was observed. Therefore in the further experiments 15 nm Al_2O_3 layers were used as plating mask. The sputtered SiN_x layer, on the other hand, was very prone to parasitic plating. With pulse plating, however, a better performance is expected for all layers. Sputtered layers would be favorable, since they can be deposited in the same tool as the TCO.

Figure 2 shows a SEM image of a NiV spot produced by LIFT. The transferred NiV is very well confined within a small area. It is advantageous to produce a well confined NiV transfer, since the size of the seed layer defines the final width of the contact fingers after plating.

The solar cells metallized by LTF and plating were produced with 15 nm ALD-Al_2O_3 as plating mask. Table 2 shows the IV measurement results of these cells compared to the results of the screen printed reference cells. The J_{SC} and FF are higher for the plated cells, which is clearly the result of the lower bulk resistivity of the plated copper, the lower finger width of 30 µm compared to the 55-60 µm wide screen printed fingers and the lower specific contact resistance of the LTF contacts. For the LTF contacts, we measured a specific contact resistance of 0.7 mΩcm², whereas the screen printed contacts reached 4 mΩcm² [19]. These differences are also reflected by the lower series resistance (R_{SER}) of the plated cells, which is also displayed in the table. An efficiency (η) of 22.2% was reached with the plated LTF cells, which corresponds to a gain of 0.5%$_{abs}$ compared to the screen printing reference. However, the number of cells produced in this first batch is low. More cells need to be produced to support the results.

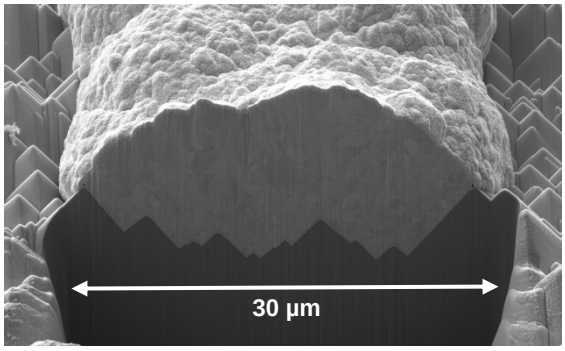

Figure 3: SEM image of a cross section of a finger produced by LTF and plating.

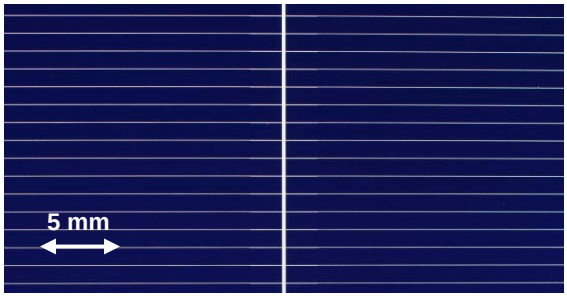

Figure 4: Photograph of a grid produced by LTF and plating.

A cross section of a plated 30 µm wide finger is visible in figure 3. As can be seen in the photograph of a plated grid in figure 4, in contrast to the results with DC-plating, there is no parasitic plating if pulse plating is used with the 15 nm Al_2O_3 layer as plating mask. As for adhesion, the plated fingers passed a tape adhesion test. However, a quantitative peel force measurement needs to be performed.

Table II: IV measurement results of two solar cells metallized by screen printing and two solar cells metallized by LTF and Cu-plating.

Metallization	Area (cm²)	V_{OC} (mV)	J_{SC} (mA/cm²)	FF (%)	R_{SER} (Ωcm²)	η (%)
Screen printing	239.0	726	37.7	79.0	0.80	21.6
Screen printing	239.0	727	37.8	79.1	0.76	21.7
LTF + Cu-plating	239.0	727	38.2	79.7	0.56	22.1
LTF + Cu-plating	239.0	728	38.0	80.1	0.47	22.2

5. CONCLUSION

With the LTF and plating approach for SHJ solar cells a maximum efficiency of 22.2% was reached, which corresponds to a gain of $0.5\%_{abs}$ compared to screen printed reference cells. Moreover, the approach is cost-effective. The laser process employs low-cost plastic foil as LIFT carrier and inexpensive ns IR lasers. The two laser steps are easily combined, because a precise alignment is not necessary. And since the dielectric plating mask remains on the cell the number of process steps is reduced. With DC-plating the ALD-Al_2O_3 plating mask showed the least parasitic plating, while the sputtered SiN_x layer was very prone to parasitic plating. With 15 nm Al_2O_3 and pulse plating no parasitic plating at all was observed. Further experiments will show whether sputtered layers, if necessary with increased thickness, will perform as well against parasitic plating, if pulse plating is used. A sputtered layer could be deposited in the same tool as the ITO, which would further simplify the production.

Even if the LTF solar cells already outperformed the screen printed reference cells in these first experiments, the process is still very likely to improve, because many parameters have not been optimized, yet. Furthermore, adhesion and module tests will show whether the produced cells can be interconnected by standard industrial soldering processes and whether the additional dielectric layer improves the module lifetime by protecting the solar cells from moisture.

6. ACKNOWLEDGEMENTS

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