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INTEGREX – PROCESS DEVELOPMENT OF A MODULE INTERCONNECTION CONCEPT FOR THIN CRYSTALLINE SILICON FILMS

Regina Pavlović, Stefan Lindekugel, Stefan Janz, Stefan Reber
Fraunhofer Institute for Solar Energy Systems
Heidenhofstraße 2, D-79102 Freiburg, Germany
Phone: +49 761 4588 5591, fax: +49 761 4588 9250
E-mail: regina.pavlovic@ise.fraunhofer.de

ABSTRACT: In this work the realization of a concept for integrated interconnected crystalline silicon thin film solar cells in a laboratory process is described. This module concept, referred to as IntegRex (Integrated interconnection of recrystallized silicon layers), is developed for recrystallized or lift-off crystalline silicon layers. Following the classical thin film approach the crystalline silicon thin film is divided into individual cell strips and interconnected monolithically on a substrate. To investigate the individual processing steps silicon on insulator (SOI) wafers with a buried oxide layer and epitaxially deposited back surface field (BSF) and base are used instead of recrystallized or lift-off crystalline silicon films.
A first batch of IntegRex mini-modules on SOI wafers was processed. Despite a not yet optimized metallization scheme, a V_{OC} of over 3 V could be reached for a mini-module consisting of five cells. Problems that occurred in the metallization process are presented here and a possible solution is discussed.
Keywords: Crystalline silicon, thin film, monolithic interconnection

1 INTRODUCTION

The IntegRex (Integrated interconnection of recrystallized silicon layers) concept aims to combine a thin-film approach with crystalline silicon wafer processing technology. Thin crystalline silicon films are separated into individual cell strips and interconnected directly on the substrate. A module detail can be seen in Fig. 1.

The module concept is developed for recrystallized [1], [2] or lift-off [3], [4] crystalline silicon films which can be processed to solar cells comparably to standard Si wafers. In this work we focus on the realization of the cell design and its optimization. Therefore, IntegRex modules on silicon on insulator (SOI) wafers were fabricated in a laboratory process which is described below. The laboratory process is developed in order to have a reliable and reproducible process for a small scale. This is important to evaluate the cell performance and parameters like e.g. cell strip width.

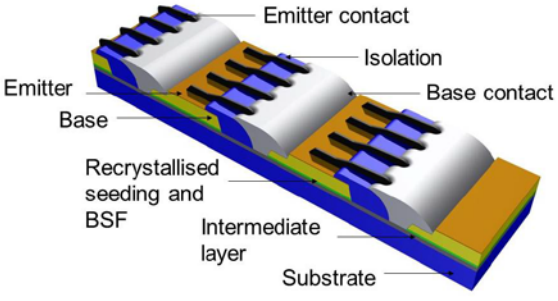

Fig. 1: Detail of integrated interconnected module with screen-printing interconnection (not to scale).

2 EXPERIMENT

Mini-modules were prepared using the processing sequence displayed in Fig. 2. In our previous publication [5] industrial processes were investigated. Here we are focusing on a laboratory process. The laboratory process involves photolithographic processing for all structuring steps and an evaporated metallization. The SOI wafers were used as reference material to evaluate the process itself. Fig. 3 shows an IntegRex on SOI module consisting of two cells with 10 mm cell strip width. In the first batch modules of 3, 5 and 10 mm cell strip width were fabricated.

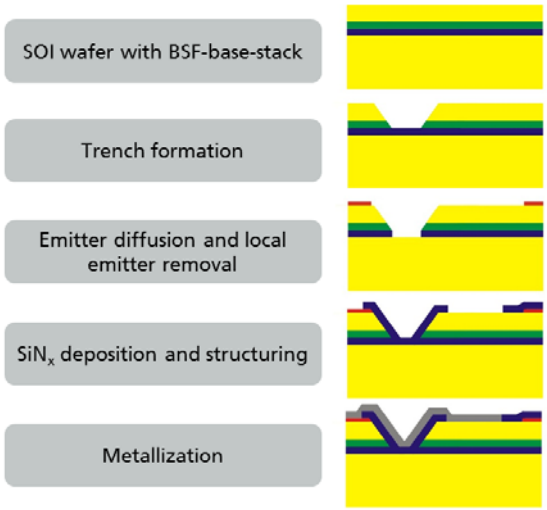

Fig. 2: Sequence of laboratory process to form integrated interconnected crystalline silicon thin-film modules. The process starts with the substrate (yellow) with SiO_2 intermediate layer (blue), back surface field (BSF) (green) and base (yellow) on top. The emitter is displayed in red, the SiN_x isolating layer in blue and the metallization is grey.

3 RESULTS

3.1 Process results

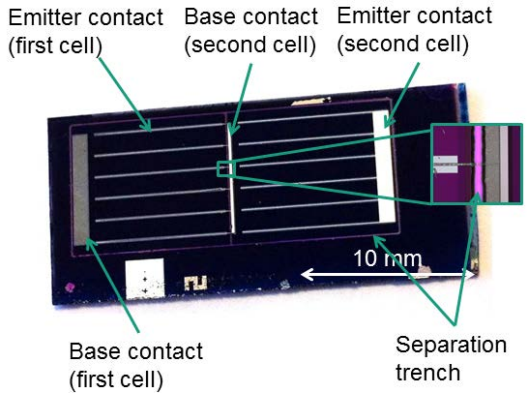

Fig. 3: Mini-module consisting of two cells with 10 mm cell width each.

Absorber preparation

As source material SOI wafers with 1.5 µm p-type Si (10 Ωcm) on top of 1 µm SiO_2 intermediate layer were used. The back surface field (BSF) and base were epitaxially deposited by atmospheric pressure chemical vapor deposition (APCVD). The 5 µm thick BSF has a boron concentration of $1 \cdot 10^{18}$ cm^{-3} and the 30 µm thick base was doped with $4 \cdot 10^{16}$ cm^{-3} boron.

Trench formation

The trenches were formed by oxide masking and KOH etching. The oxide mask was structured in a photolithographic process with hydrofluoric acid. The trenches were then etched in 8 % aqueous KOH at 80%.

Emitter diffusion and local emitter removal

A 40 Ω/□ emitter was diffused from $POCl_3$ to get a high surface concentration as well as a deep pn-junction. These are needed to contact the emitter of the module with aluminum. The high surface concentration enables the contact formation between silicon and aluminum and the deep pn-junction prevents shunting of the cells by aluminum spikes through the emitter.

As all contacting is done on the front side of the cell, the emitter needs to be structured to get access to the base. The structuring of the emitter was carried out by masking with photoresist and plasma etching in a SF_6 plasma.

Silicon nitride deposition and structuring

As the emitter structuring leaves an open pn-junction near the trench edge and the metallization runs over the trench, the open pn-junction needs to be isolated from the metallization. Silicon nitride (SiN_x) was chosen as isolating layer since it can simultaneously serve as anti-reflection coating and passivation layer and isolate the pn-junction from the evaporated metallization. A 70 nm thick layer was deposited by plasma enhanced chemical vapor deposition (PECVD). To enable contact formation in the areas of emitter and base contact the SiN_x layer was structured with aqueous hydrofluoric acid through a photoresist mask.

Metallization

To contact emitter and base with the same metal we chose aluminum as contacting material. On a structured photoresist a stack of Al/Ti/Pd/Ag was evaporated. After lift-off, the metallization was to be thickened by silver electro-plating and later sintered for better contact formation.

As can be seen in Fig. 4a) the metallization was interrupted in the trench, and could therefore not be electroplated. After manual application of conductive silver, electro-plating was possible, see Fig. 4b). During electro-plating adhesion problems occurred and fingers peeled off. The samples were then sintered for 10 min at 350 °C to enhance contact adhesion, before further thickening of the contacts. In this manner all mini-modules could be electro-plated, but most of them exhibit at least partly peeled off contacts.

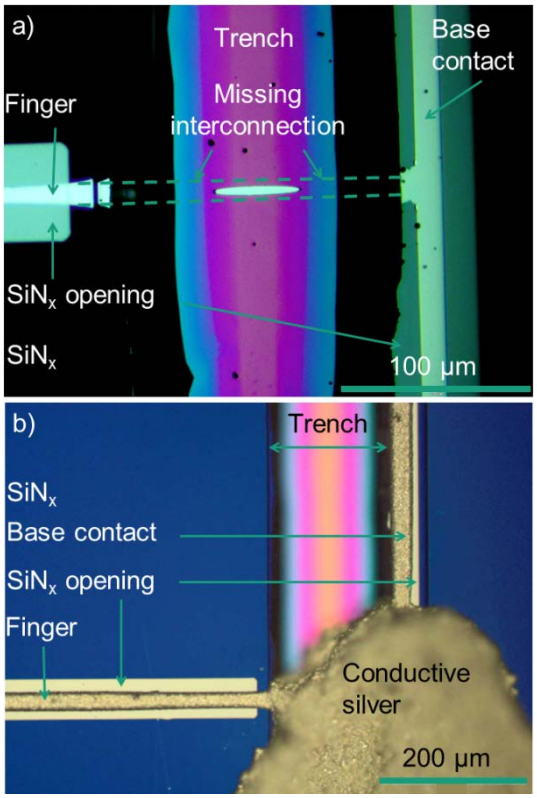

Fig. 4: Interconnection between two neighboring cell strips. Emitter contact is running from the left over the trench to connect to base contact of the next cell on the right. a) Interconnection in the trench is missing. b) Interconnection established by conductive silver, afterwards electro-plating is possible.

3.2 Solar cell results

The IV characteristics of the fabricated mini-modules were measured and are displayed in Tab. 1. The area for the efficiency calculation includes the trenches between the cells. The contacting pads for the measurement were not included as these could lie under the module frame. The best IntegRex on SOI module so far exhibits an efficiency of 8.8 %.

With a 30 µm thick base and no texture the short circuit current (J_{SC}) lies in the expected range with values up to 27.5 mA. As the cells are interconnected serially, the open circuit voltages (V_{OC}) of the cells add up to the V_{OC} of the module. It is clearly visible from the IV

measurements that the interconnection of the cells was successful and it can be concluded that each cell has an average V_{OC} of 600 mV. The best IntegRex on SOI mini-module has an average V_{OC} of 620 mV per cell. One mini-module consisting of five cells achieved a V_{OC} of over 3 V.

The IV characteristics show an increased series resistance (R_S) for all mini-modules, which can partly be attributed to problems with the metallization described above. The raised R_S leads to a decreased fill factor (FF). The expected dependence of R_S and FF on the cell strip width can consequently not be seen in these results.

Tab. 1: IV parameters of IntegRex on SOI modules.

Cell width (mm)	Number of cells	V_{OC} (mV)	J_{SC} (mA/cm²)	FF (%)	η (%)
3	2	1229	26.3	31	4.9
5	2	1240	27.5	52	8.8
10	2	1132	22.4	37	4.7
5	5	3055	27.3	53	8.7
10	4	2494	24.2	38	5.6

4 OPTIMIZATION OF METALLIZATION STEPS

To determine the origin of the interrupted interconnection, samples with etched trenches were spin-coated with photoresist. In Fig. 5 a microscopy image of the cross section of such a sample is shown. At the bottom of the trench, the photoresist piles up in the corners due to the spin-coating process.

As a positive resist was used for the metallization, the thick areas in the trench corners were likely not completely exposed and therefore not developed. Subsequently the metal is evaporated onto the residual resist and, during the lift-off, the metal in the trench corners is lifted off as well.

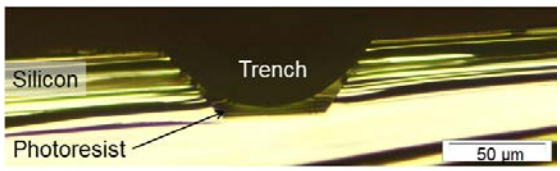

Fig. 5: Microscopy image of cross section of sample with etched trenches after spin-coating of photoresist.

In order to get a continuous interconnection the resist has to be completely removed during development. Exposure with parameters that would completely expose a positive resist in the trench corners, would lead to overexposing the thinner parts of the resist.

A negative resist on the other hand does not have to be exposed for a longer time but developed longer. The longer development increases the undercut of the resist. As the next step is the evaporation of metal the undercut is not crucial here.

In Fig. 6a) a microscopy image of a sample with trenches and negative photoresist after exposure and development is displayed. The undercut in the trench is clearly visible. Fig. 6b) shows the sample after metal evaporation and lift-off. The metal finger runs through the trench without disconnections in the trench corners. After these pre-tests we are confident to have found a solution resolving the disconnection problem during the metallization.

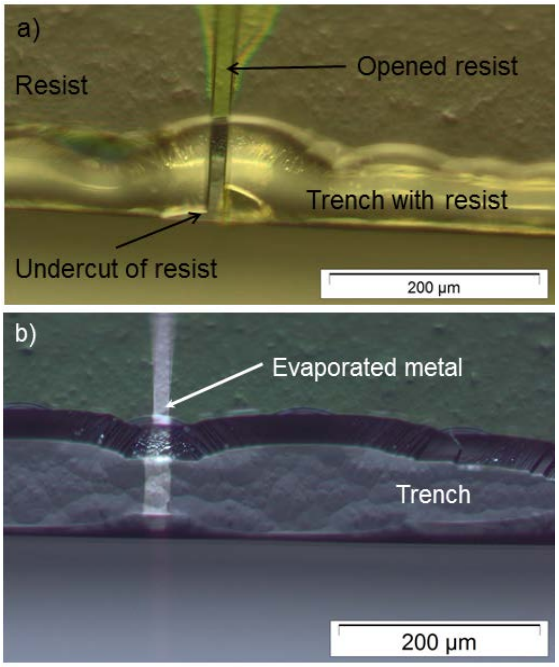

Fig. 6: Microscopy image of tilted sample with etched trenches, view perpendicular to the flank of a trench. a) Sample with negative photoresist after exposure and development. b) Sample after evaporation of metal and lift-off of resist.

5 SUMMARY AND CONCLUSION

A laboratory process for the realization of the integrated interconnection of crystalline silicon thin film (cSi-TF) solar cells according to the IntegRex concept was presented. First IntegRex modules on SOI wafers were fabricated successfully. In spite of metallization problems, an IntegRex on SOI module with 5 cells reached a V_{OC} over 3 V.

Issues in the metallization process originate from the spin-coating and further processing of the used photoresist. A possible solution was found by using a negative resist. First pre-tests with a negative resist were carried out with promising results. Microscopy pictures showed that the resist could be developed even in the trench corners and metal was evaporated continuously through the whole trench.

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